FIG. 1

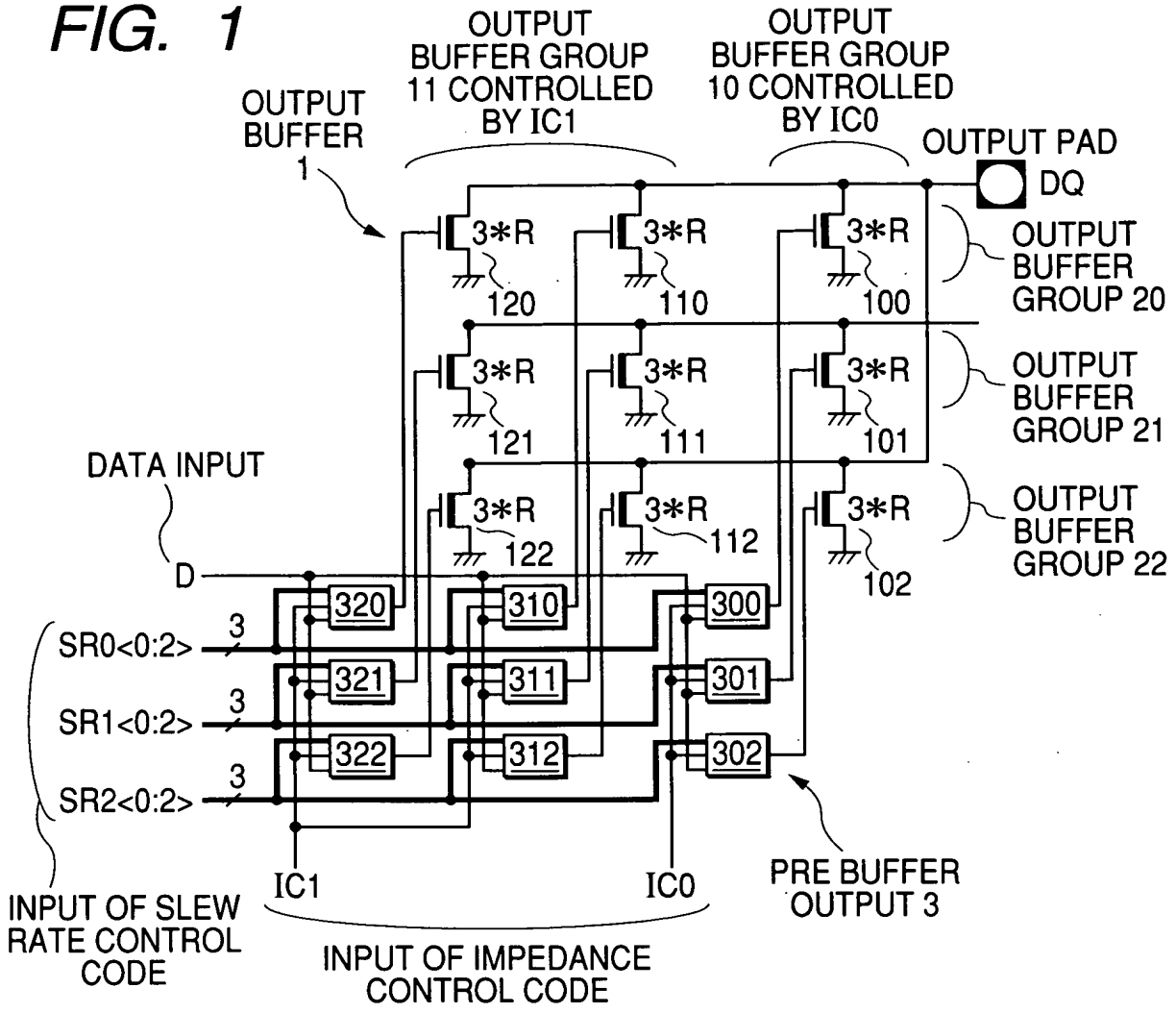

OUTPUT BUFFER 1
OUTPUT BUFFER GROUP 11 CONTROLLED BY IC1
OUTPUT BUFFER GROUP 10 CONTROLLED BY IC0
OUTPUT PAD
DQ
3*R
120
110
100
OUTPUT BUFFER GROUP 20
121
111
101
OUTPUT BUFFER GROUP 21
122
112
102
OUTPUT BUFFER GROUP 22
DATA INPUT
D
320
310
300
SR0<0:2>
3
321
311
301
SR1<0:2>
322
312
302
SR2<0:2>
IC1
IC0
PRE BUFFER OUTPUT 3
INPUT OF SLEW RATE CONTROL CODE
INPUT OF IMPEDANCE CONTROL CODE

FIG. 2

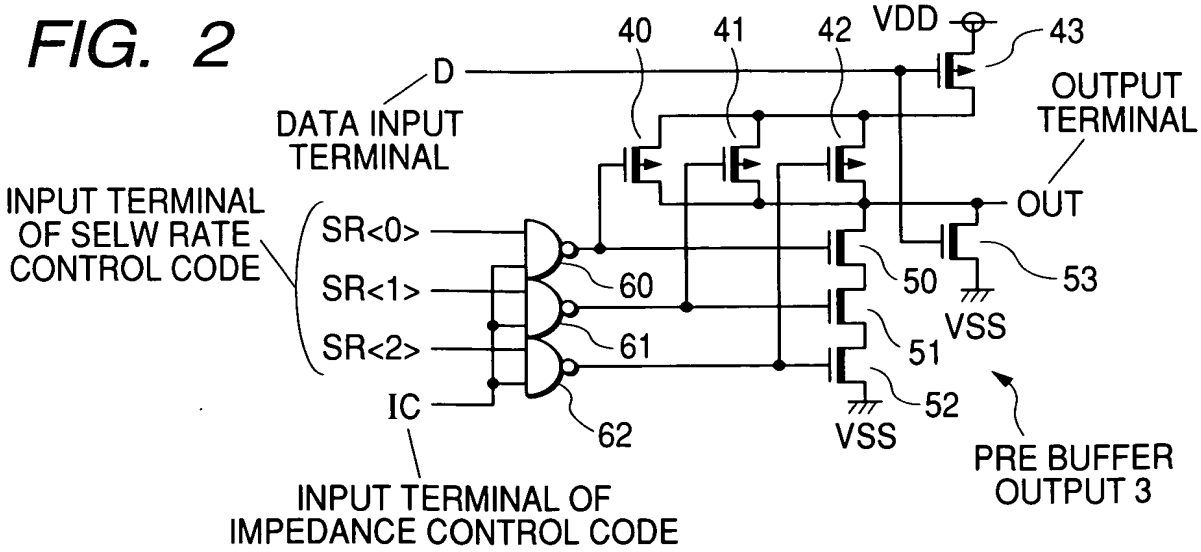

D
DATA INPUT TERMINAL
40
41
42
VDD
43
OUTPUT TERMINAL
OUT
INPUT TERMINAL OF SELW RATE CONTROL CODE
SR<0>
SR<1>
SR<2>
60
61
62
IC
50
51
52
53
VSS
VSS
PRE BUFFER OUTPUT 3
INPUT TERMINAL OF IMPEDANCE CONTROL CODE

FIG. 3

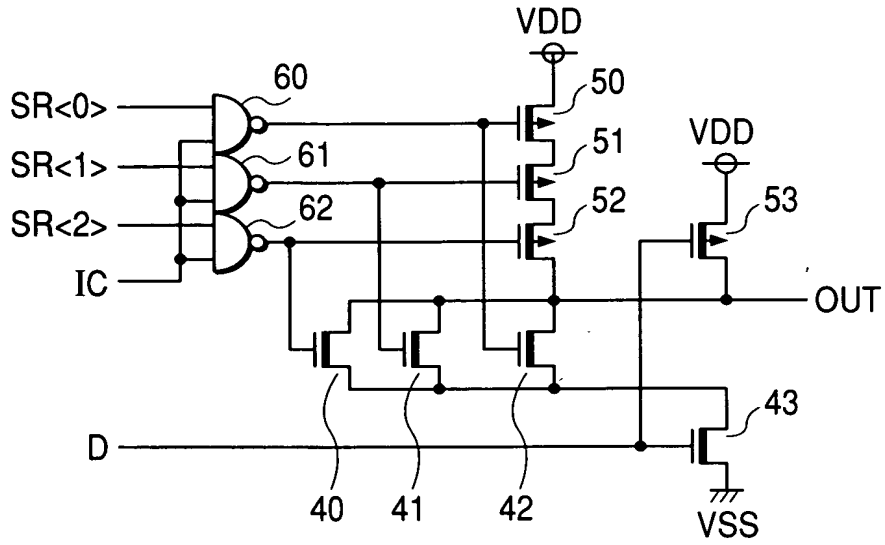


FIG. 4

IMPEDANCE CODE		OPERATING BUFFERS		DQ IMPEDANCE
IC1	IC0		(NUMBER)	
0	0	NONE	0	∞
0	1	100～102	3	R
1	0	110～122	6	R/2
1	1	100～122	9	R/3

FIG. 5

SLEW RATE CODE			PMOS WHICH ARE ON STATE	ON RESISTANCE OF PRE BUFFERS	OUTPUT SLEW RATE
SR<2>	SR<1>	SR<0>			
1	1	1	40~42	SMALL	BIG
1	1	0	40,41	↑	↑
1	0	1	40,42	↕	↕
1	0	0	40	↕	↕
0	1	1	41,42	↕	↕
0	1	0	41	↓	↓
0	0	1	42	BIG	SMALL
0	0	0	NONE	∞(PROHIBIT)	–

FIG. 6

BUFFER GROUPS CONTROLLED BY SLEW RATE	IMPEDANCE CODE COMBINATION (IC1,IC0)			
	0,0	0,1	1,0	1,1
20	∞	3*R	1.5*R	R
21	∞	3*R	1.5*R	R
22	∞	3*R	1.5*R	R
TOTAL	∞	R	R/2	R/3

FIG. 7

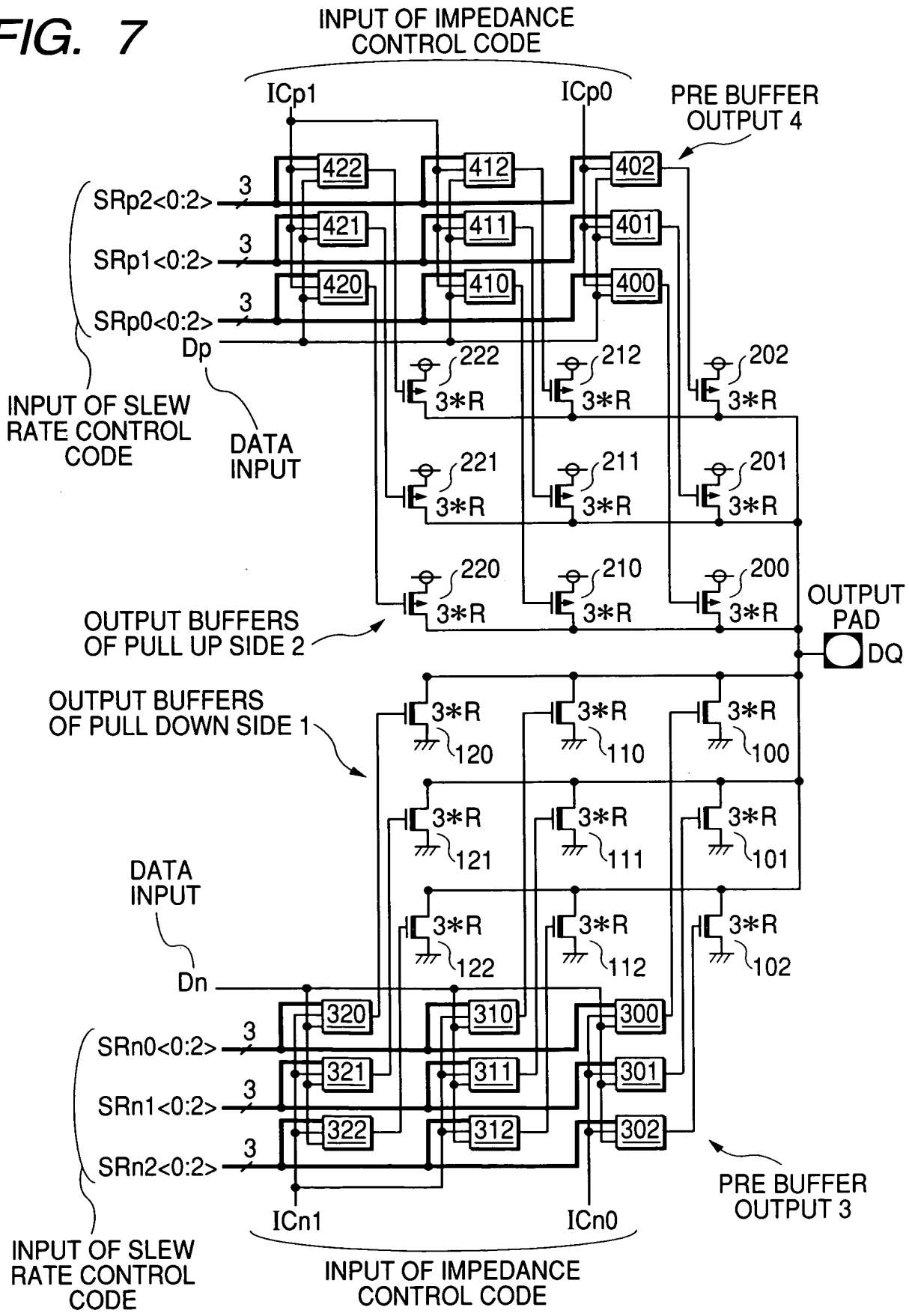

INPUT OF IMPEDANCE CONTROL CODE
ICp1
ICp0
PRE BUFFER OUTPUT 4
422
412
402
421
411
401
420
410
400
SRp2<0:2>
SRp1<0:2>
SRp0<0:2>
3
Dp
222
212
202
221
211
201
220
210
200
3*R
INPUT OF SLEW RATE CONTROL CODE
DATA INPUT
OUTPUT BUFFERS OF PULL UP SIDE 2
OUTPUT PAD
DQ
OUTPUT BUFFERS OF PULL DOWN SIDE 1
120
110
100
121
111
101
122
112
102
DATA INPUT
Dn
320
310
300
321
311
301
322
312
302
SRn0<0:2>
SRn1<0:2>
SRn2<0:2>
PRE BUFFER OUTPUT 3
ICn1
ICn0
INPUT OF SLEW RATE CONTROL CODE
INPUT OF IMPEDANCE CONTROL CODE

FIG. 8

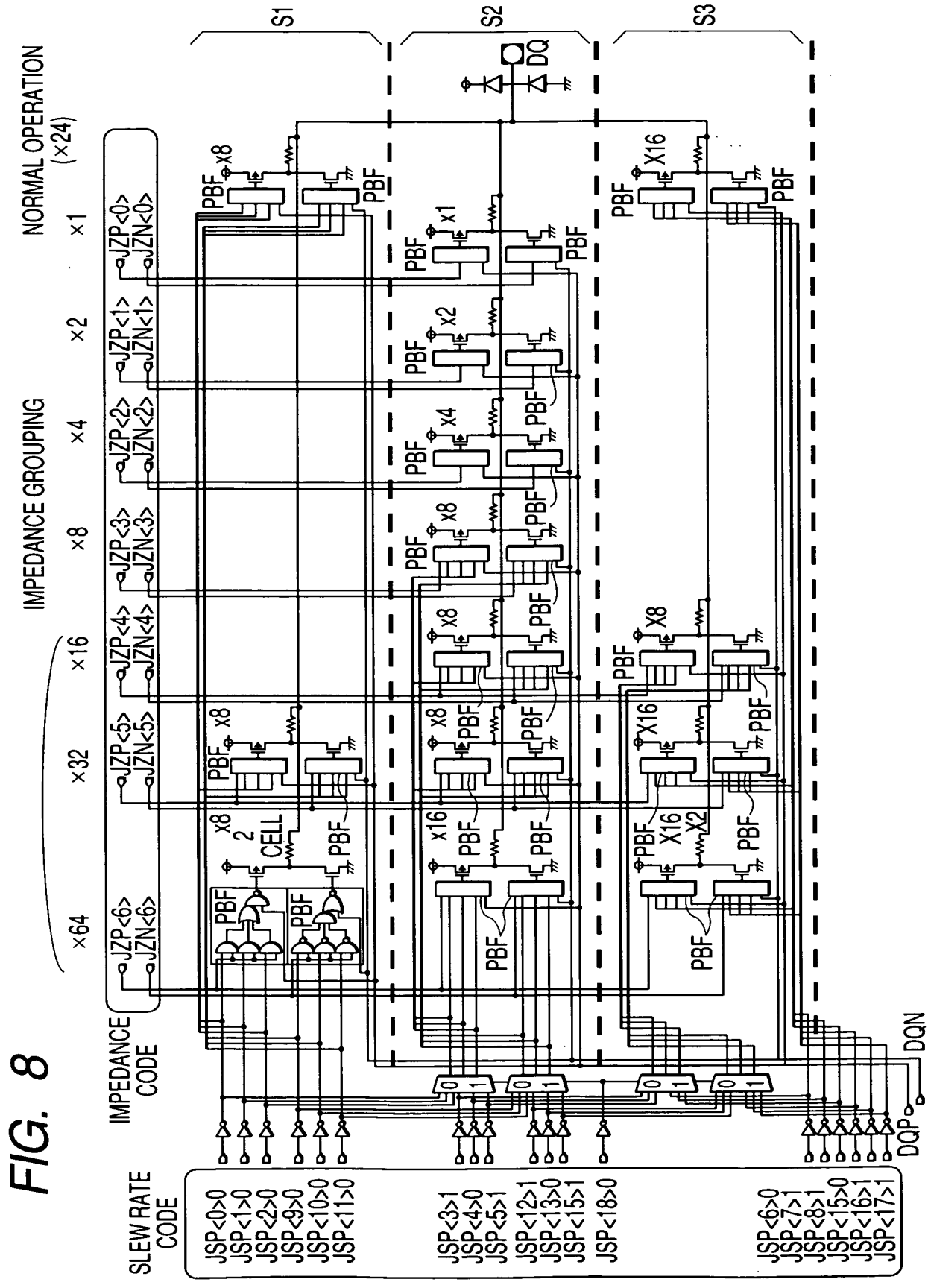

NORMAL OPERATION
(×24)
IMPEDANCE GROUPING
×1
×2
×4
×8
×16
×32
×64
JZP<0>
JZN<0>
JZP<1>
JZN<1>
JZP<2>
JZN<2>
JZP<3>
JZN<3>
JZP<4>
JZN<4>
JZP<5>
JZN<5>
JZP<6>
JZN<6>
IMPEDANCE CODE
SLEW RATE CODE
S1
S2
S3
DQ
DQP
DQN
PBF
x8
x1
x2
x4
x16
X16
X8
X2
CELL
JSP<0>0
JSP<1>0
JSP<2>0
JSP<9>0
JSP<10>0
JSP<11>0
JSP<3>1
JSP<4>0
JSP<5>1
JSP<12>1
JSP<13>0
JSP<15>1
JSP<18>0
JSP<6>0
JSP<7>1
JSP<8>1
JSP<15>0
JSP<16>1
JSP<17>1

FIG. 9

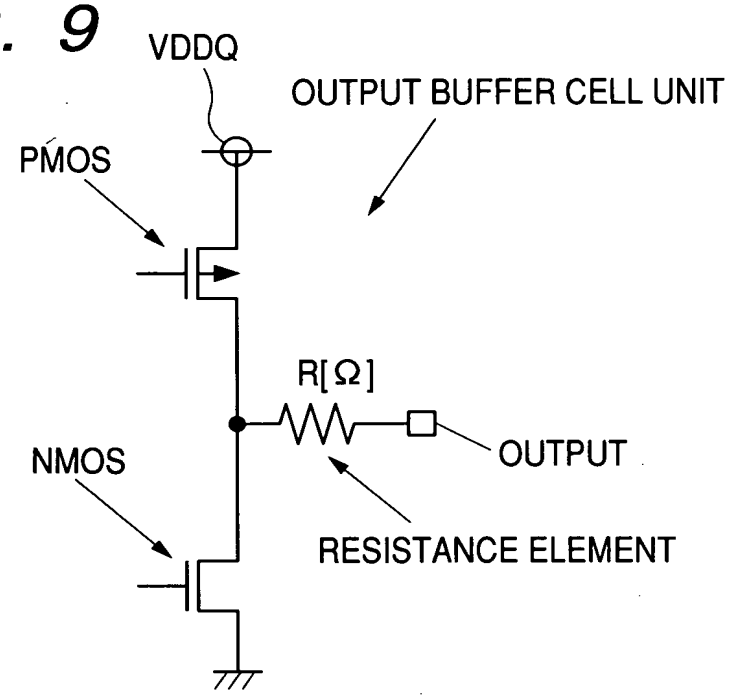

VDDQ
OUTPUT BUFFER CELL UNIT
PMOS
R[Ω]
OUTPUT
NMOS
RESISTANCE ELEMENT

FIG. 10

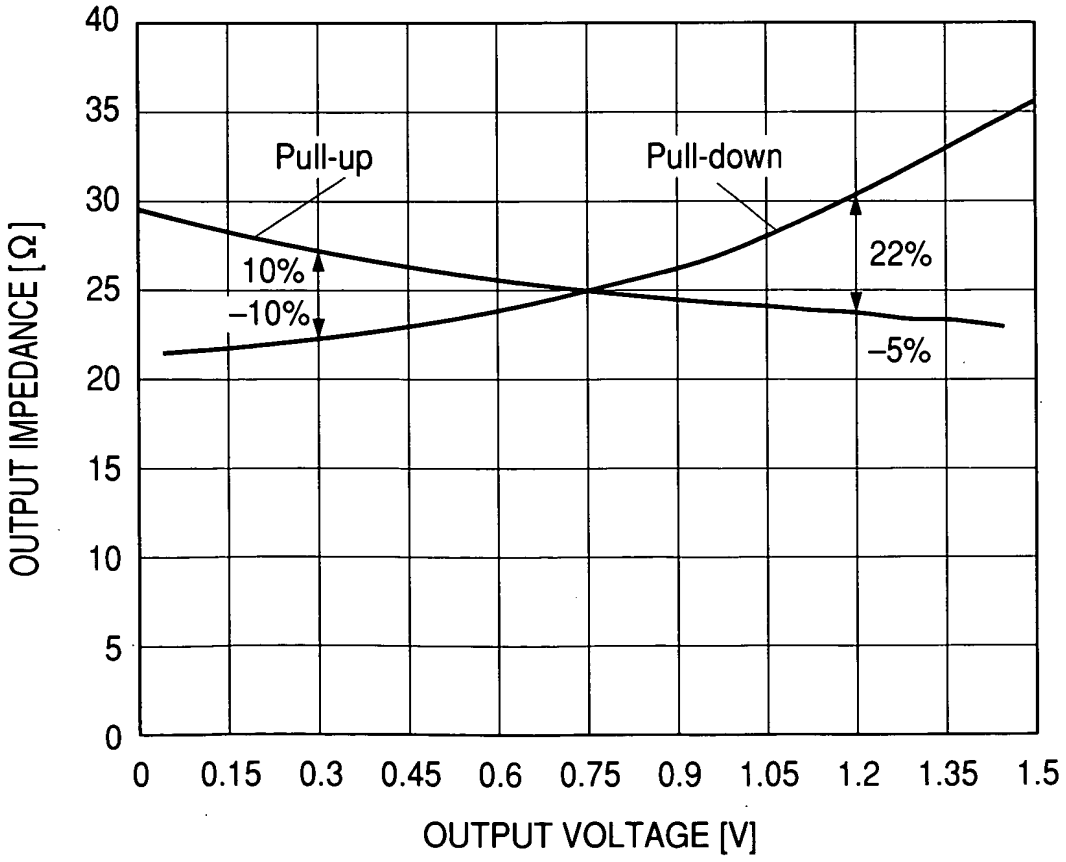

40
35
30
25
20
15
10
5
0
Pull-up
Pull-down
10%
−10%
22%
−5%
OUTPUT IMPEDANCE [Ω]
0
0.15
0.3
0.45
0.6
0.75
0.9
1.05
1.2
1.35
1.5
OUTPUT VOLTAGE [V]

FIG. 11

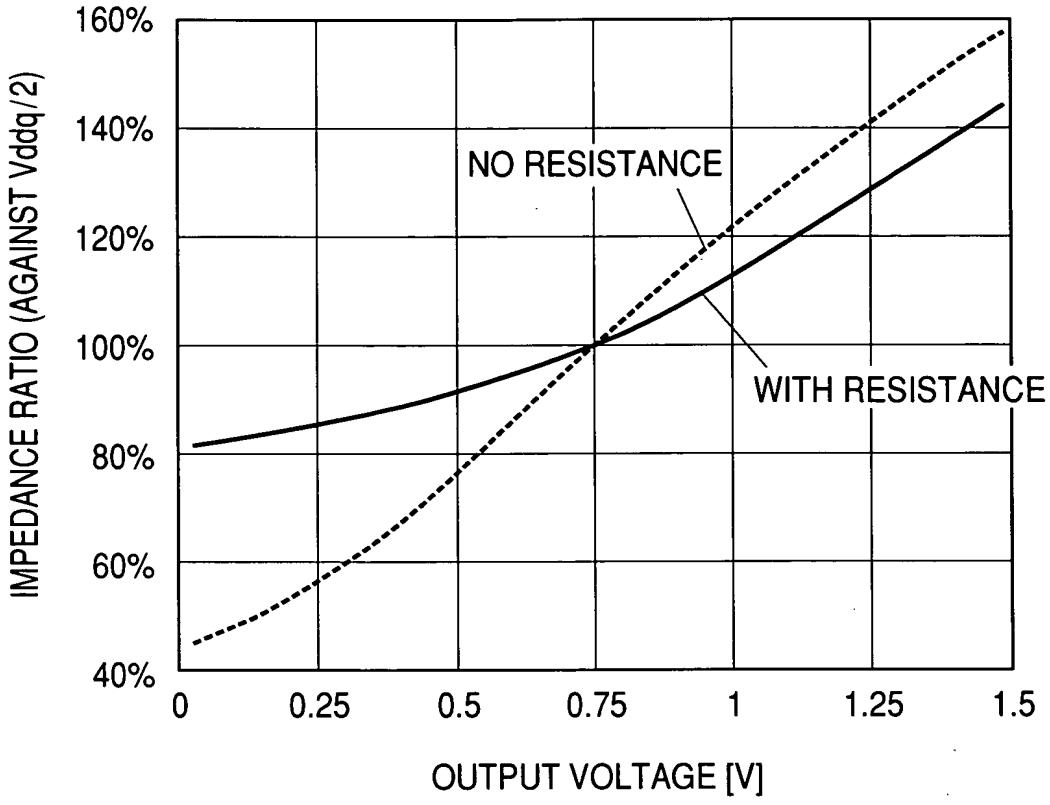

160%
140%
120%
100%
80%
60%
40%
IMPEDANCE RATIO (AGAINST Vddq/2)
NO RESISTANCE
WITH RESISTANCE
0
0.25
0.5
0.75
1
1.25
1.5
OUTPUT VOLTAGE [V]

FIG. 12

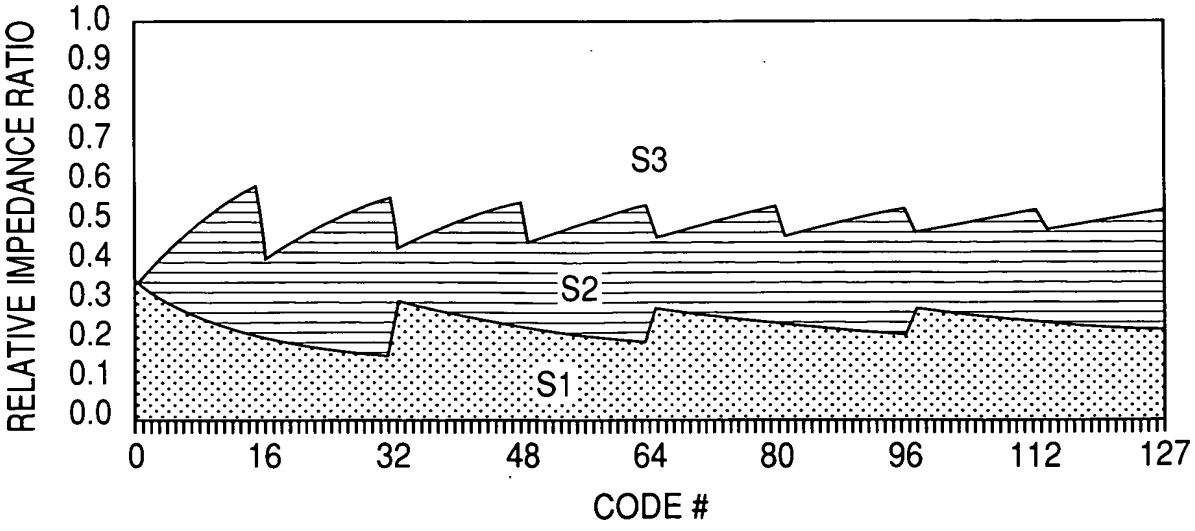

1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
RELATIVE IMPEDANCE RATIO
S3
S2
S1
0
16
32
48
64
80
96
112
127
CODE #

FIG. 13

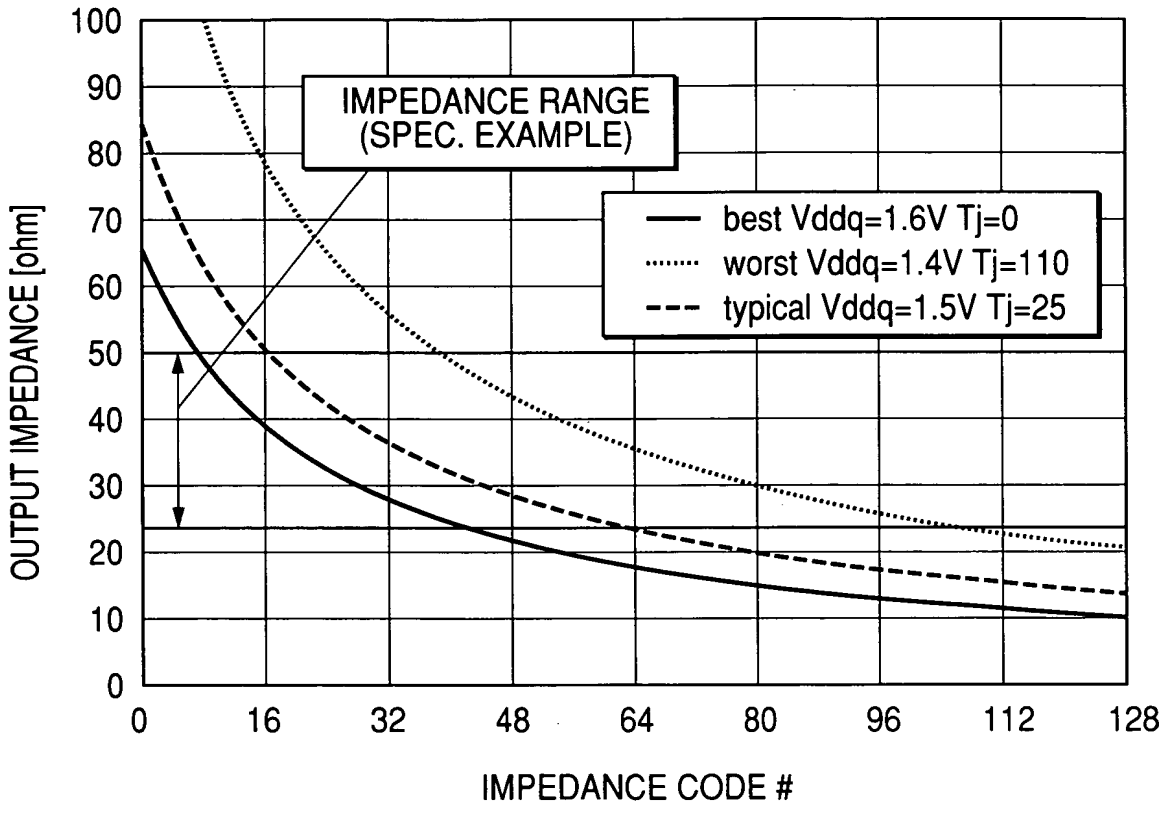

IMPEDANCE RANGE
(SPEC. EXAMPLE)
best Vddq=1.6V Tj=0
worst Vddq=1.4V Tj=110
typical Vddq=1.5V Tj=25
OUTPUT IMPEDANCE [ohm]
IMPEDANCE CODE #
0
10
20
30
40
50
60
70
80
90
100
0
16
32
48
64
80
96
112
128

FIG. 14

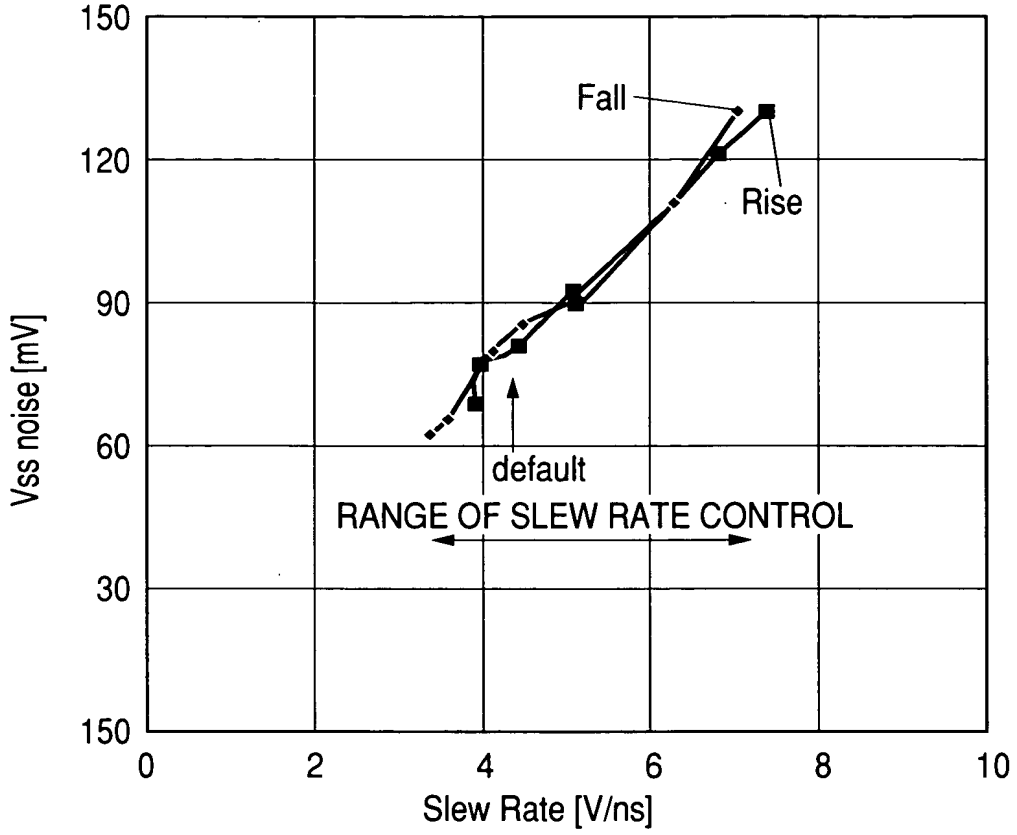

150
120
90
60
30
150
Vss noise [mV]
Fall
Rise
default
RANGE OF SLEW RATE CONTROL
0
2
4
6
8
10
Slew Rate [V/ns]

FIG. 15

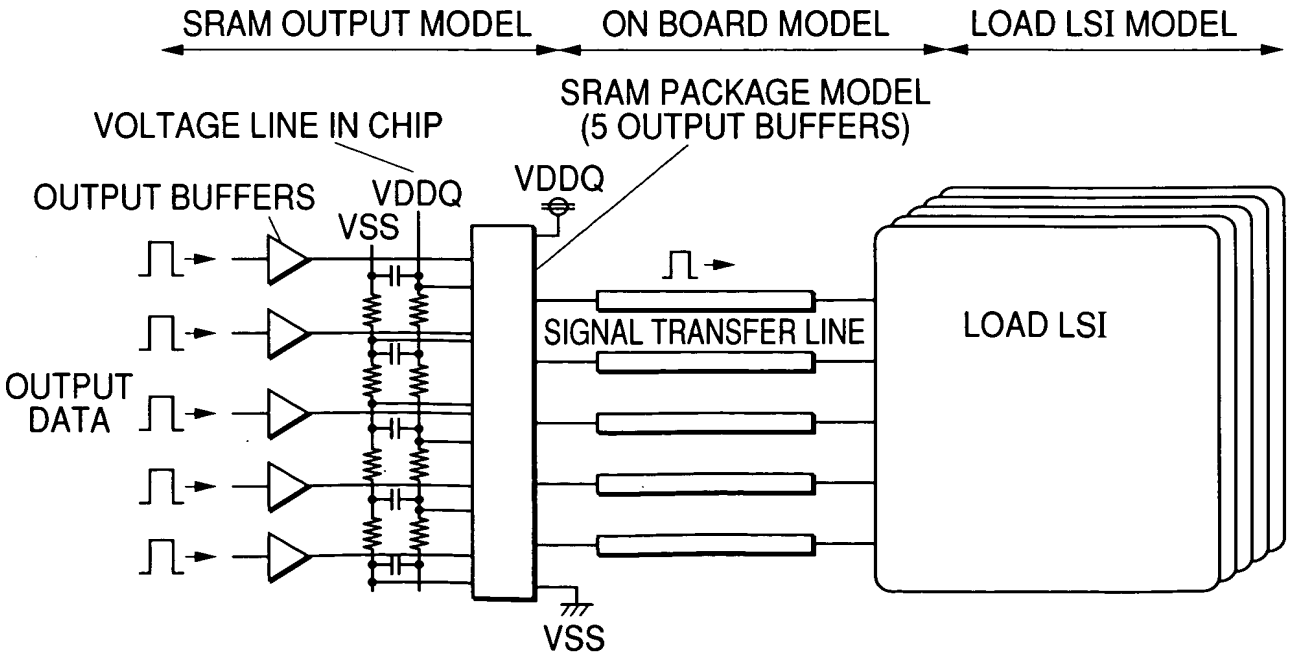

SRAM OUTPUT MODEL
ON BOARD MODEL
LOAD LSI MODEL
SRAM PACKAGE MODEL
(5 OUTPUT BUFFERS)
VOLTAGE LINE IN CHIP
OUTPUT BUFFERS
VDDQ
VSS
VDDQ
SIGNAL TRANSFER LINE
LOAD LSI
OUTPUT
DATA
VSS

FIG. 16(a)

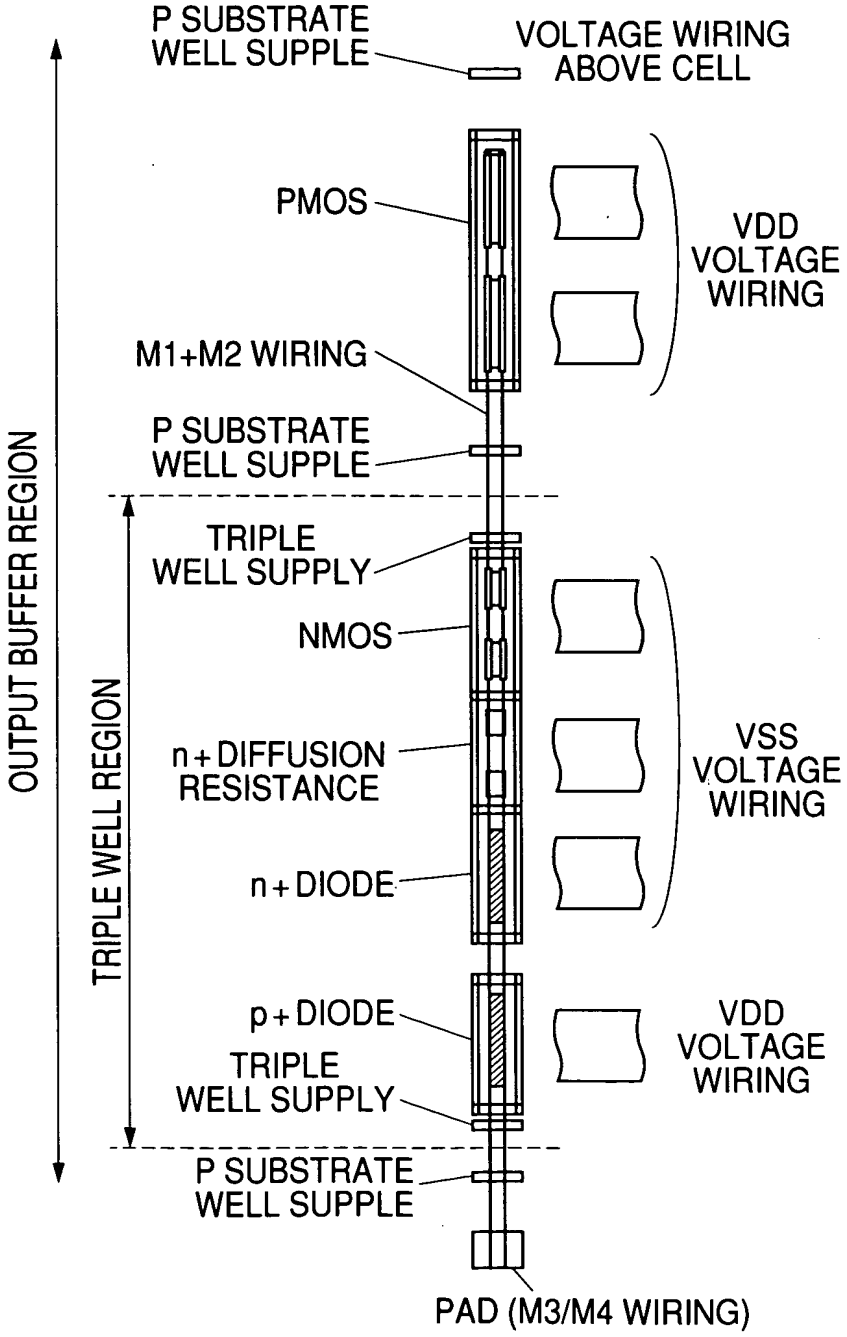


FIG. 16(b)

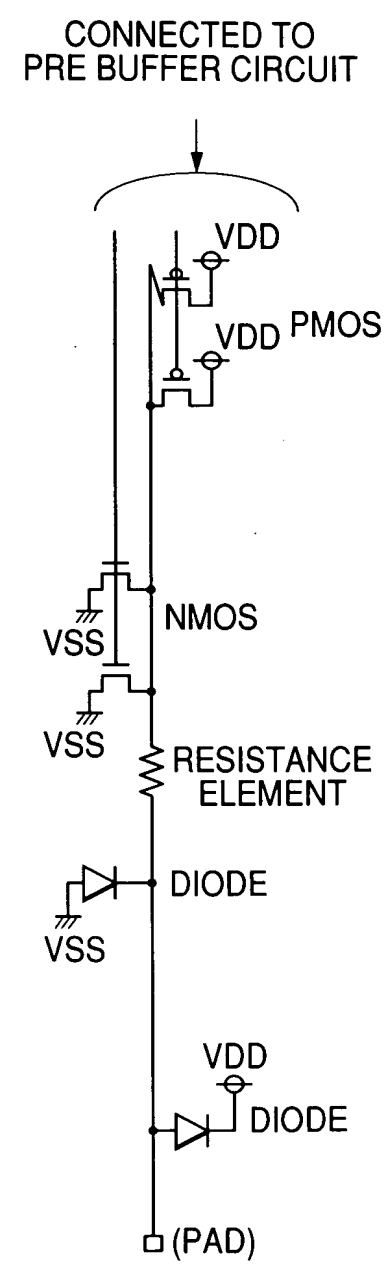


FIG. 17

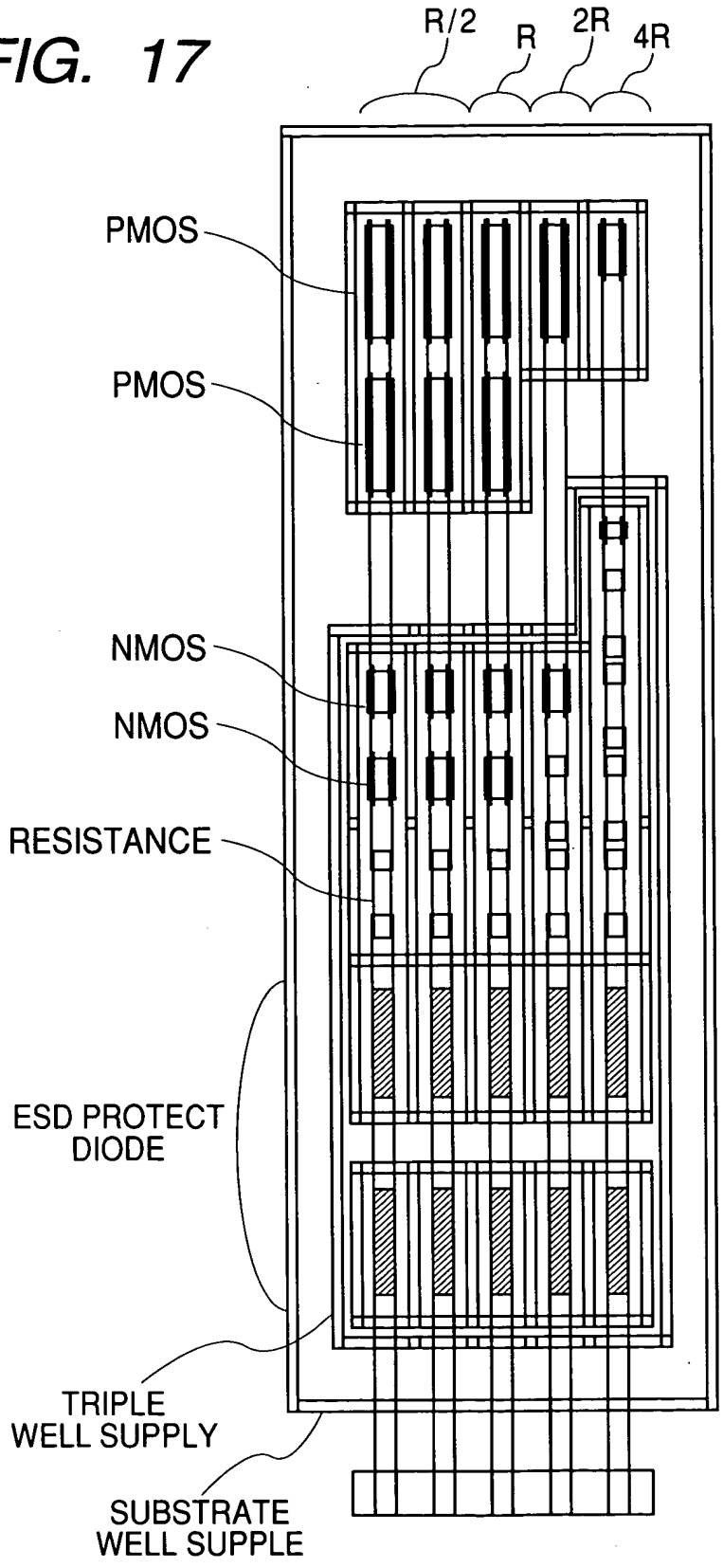

R/2
R
2R
4R
PMOS
PMOS
NMOS
NMOS
RESISTANCE
ESD PROTECT DIODE
TRIPLE WELL SUPPLY
SUBSTRATE WELL SUPPLE

FIG. 18

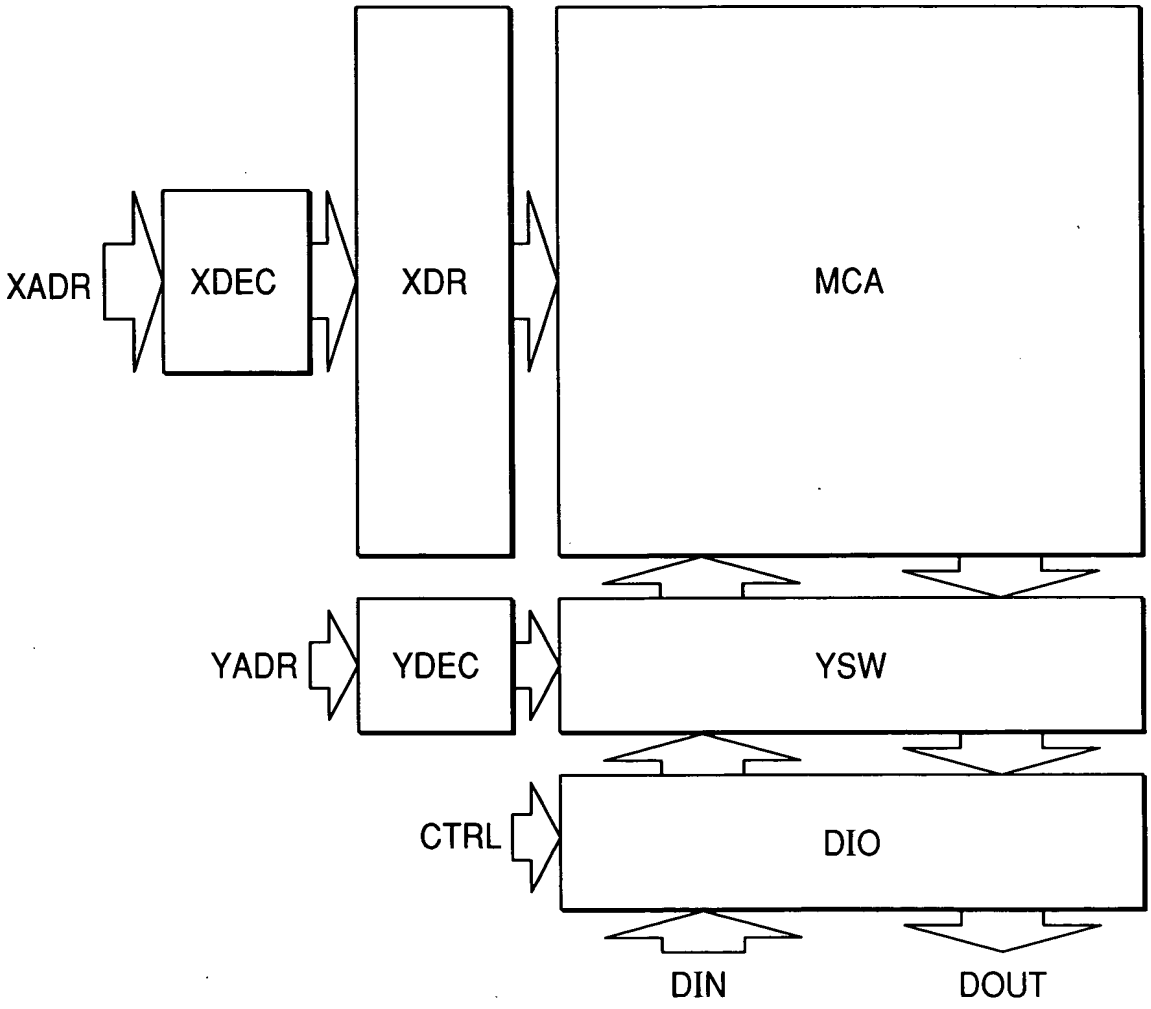


FIG. 19

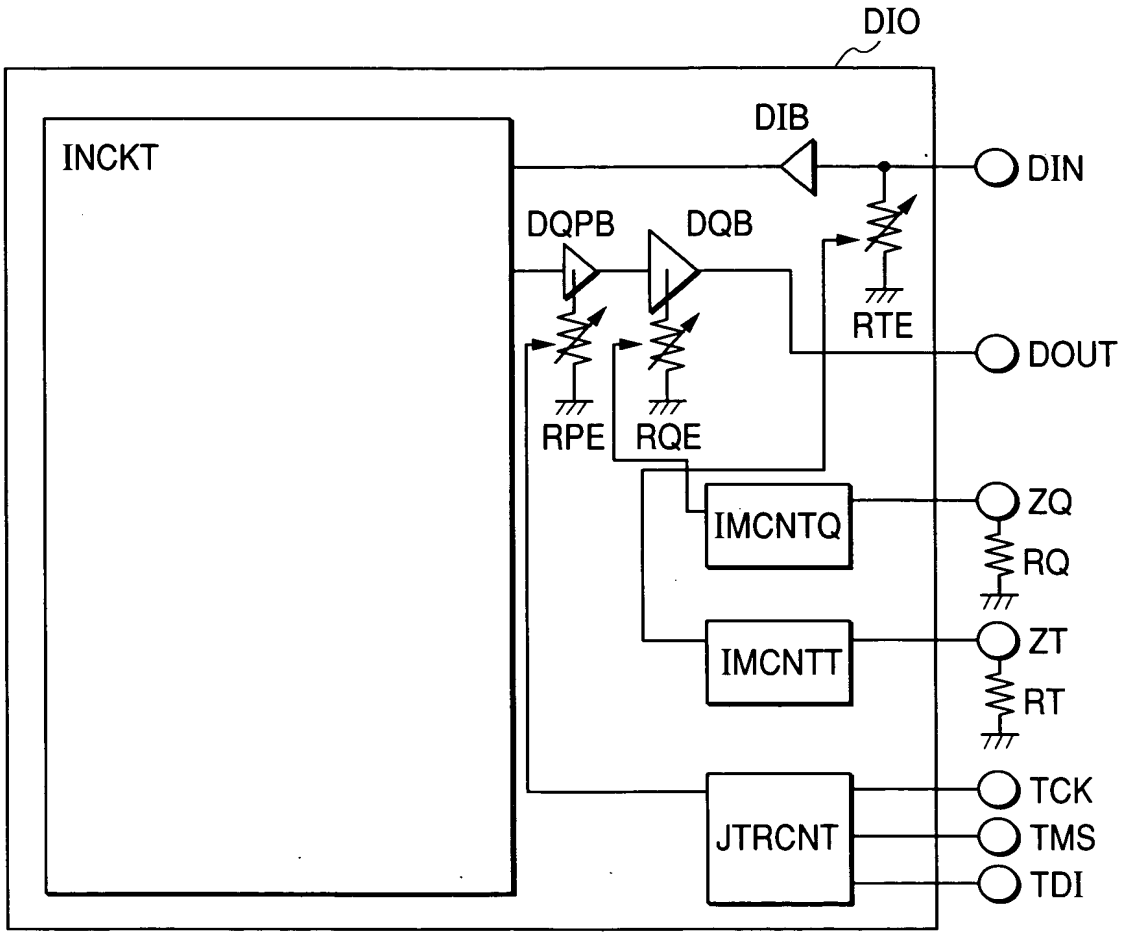

DIO
INCKT
DIB
DIN
DQPB
DQB
RTE
DOUT
RPE
RQE
IMCNTQ
ZQ
RQ
IMCNTT
ZT
RT
JTRCNT
TCK
TMS
TDI

FIG. 20

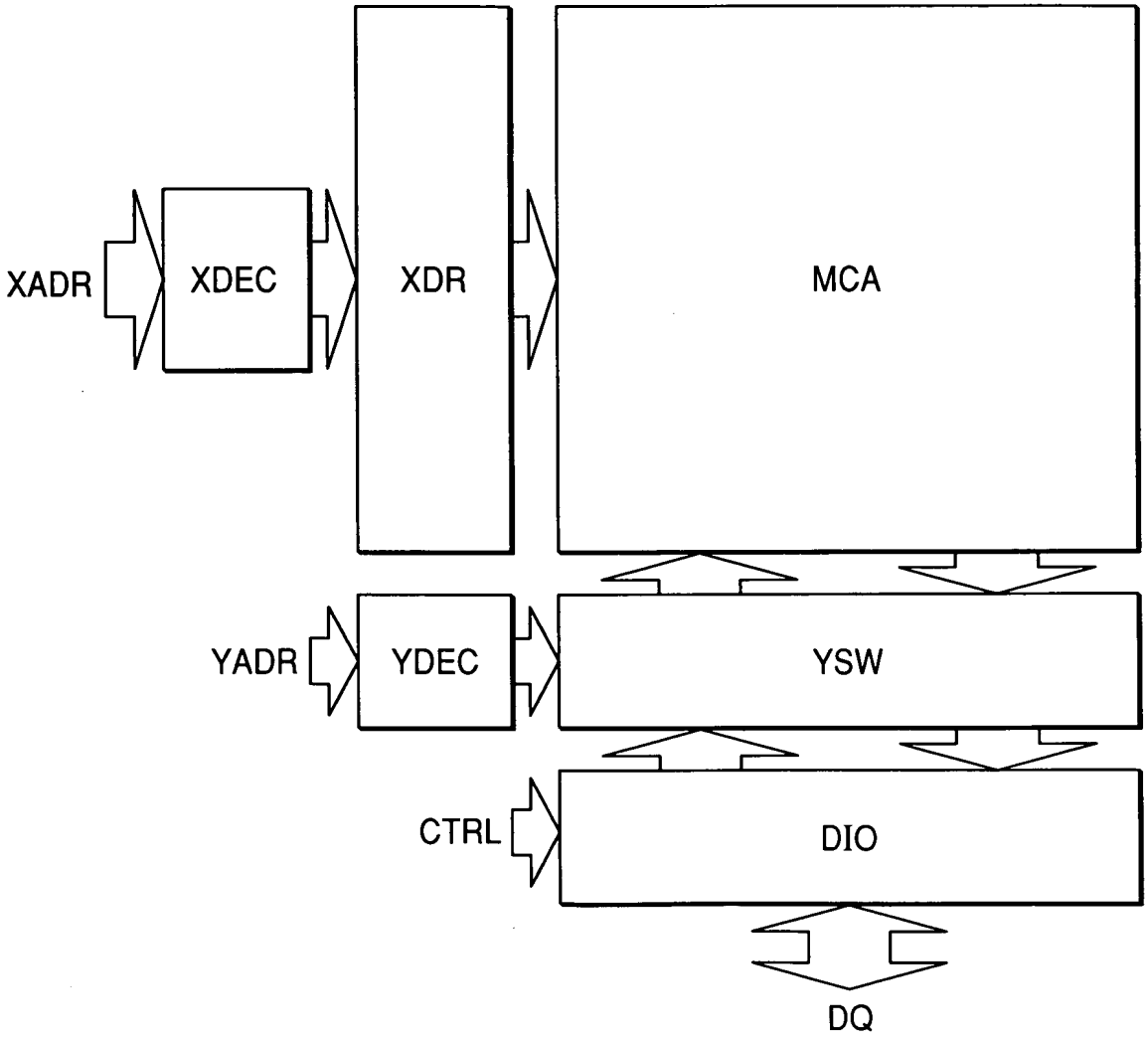


FIG. 21

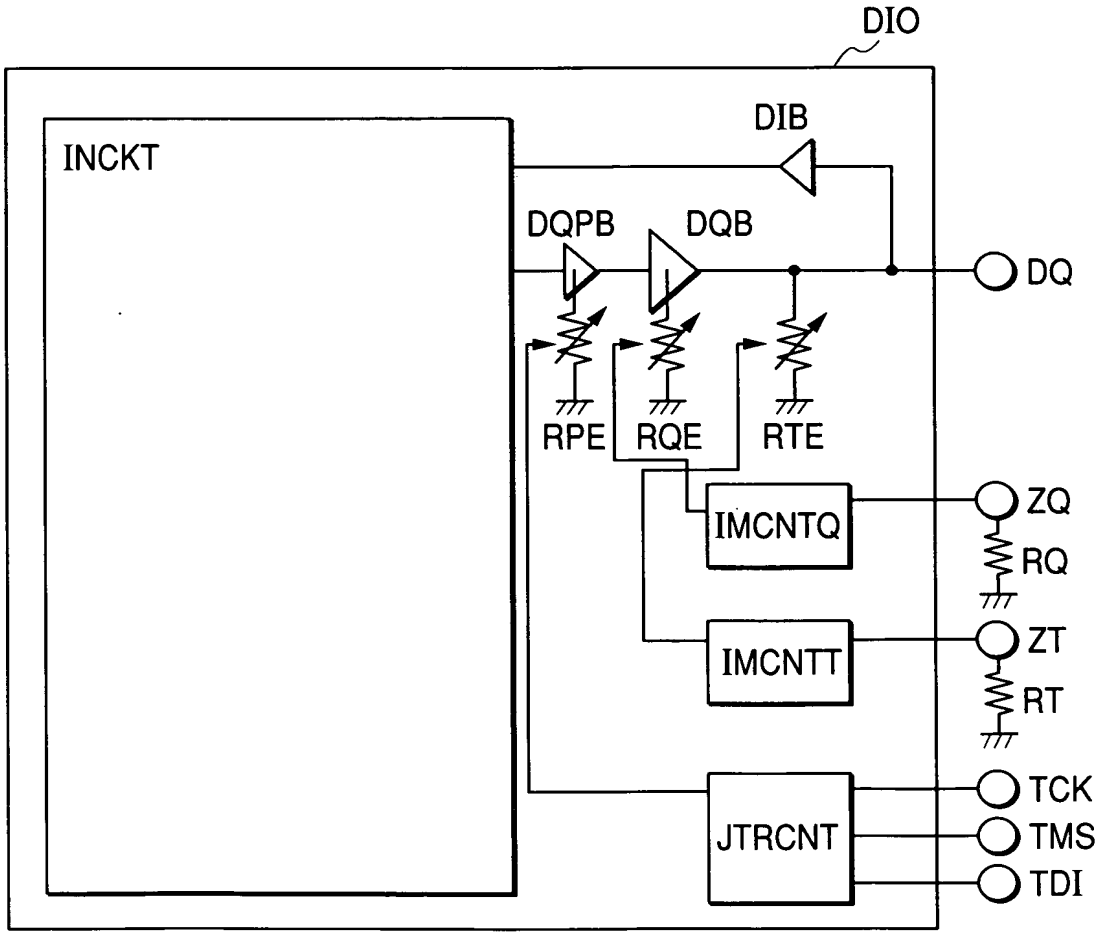

DIO
INCKT
DIB
DQPB
DQB
DQ
RPE
RQE
RTE
IMCNTQ
ZQ
RQ
IMCNTT
ZT
RT
JTRCNT
TCK
TMS
TDI

FIG. 22

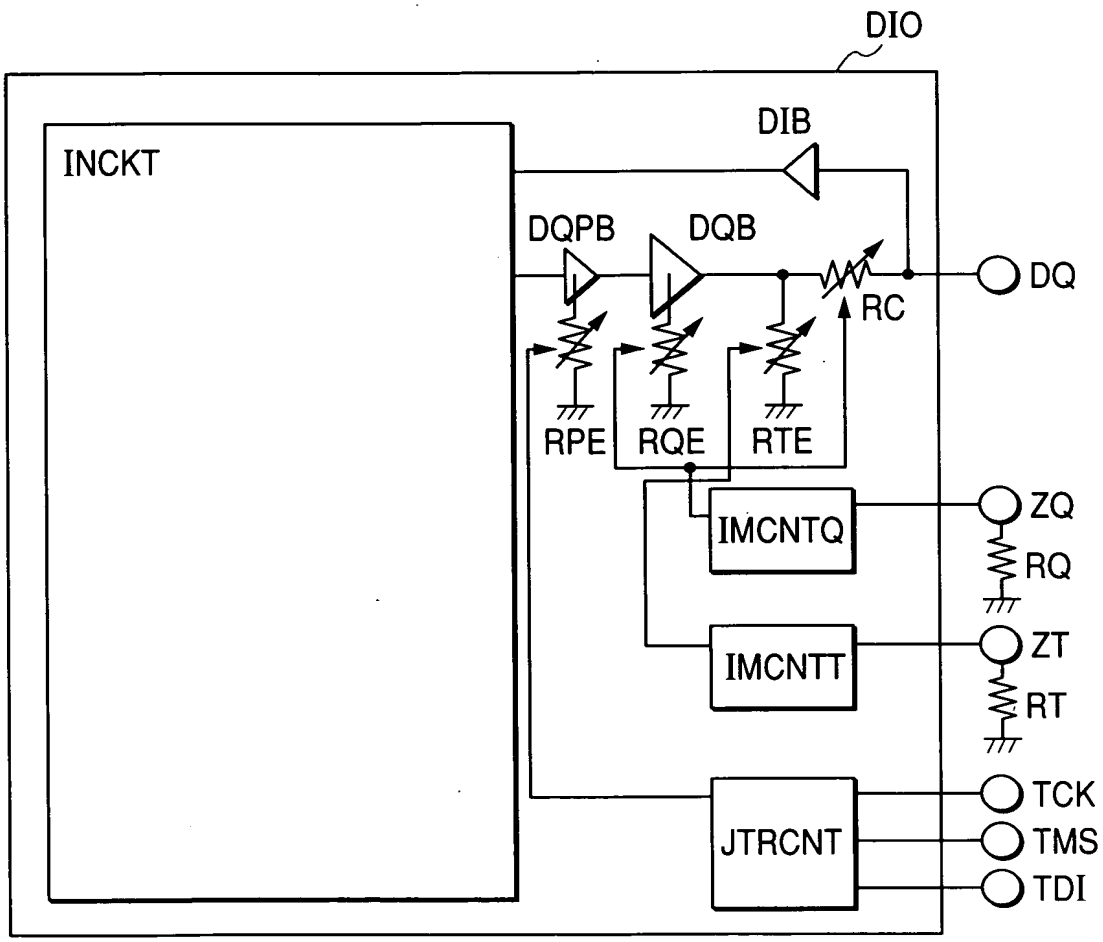

DIO
INCKT
DIB
DQPB
DQB
DQ
RC
RPE
RQE
RTE
IMCNTQ
ZQ
RQ
IMCNTT
ZT
RT
JTRCNT
TCK
TMS
TDI

FIG. 23

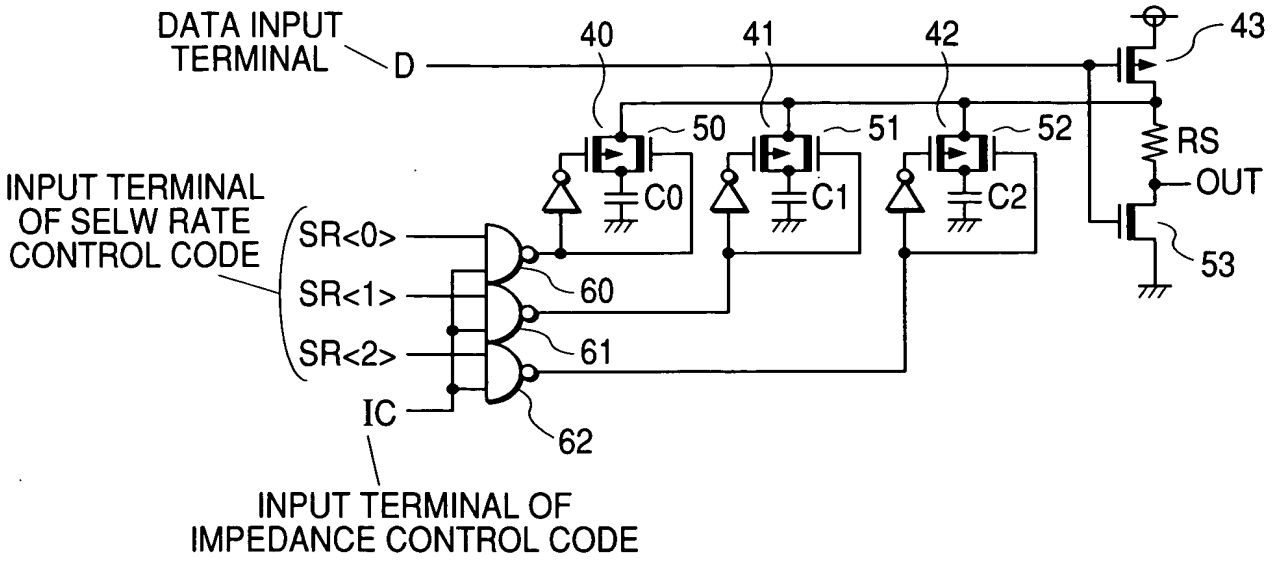

DATA INPUT TERMINAL
D
40
41
42
43
50
51
52
C0
C1
C2
RS
OUT
53
INPUT TERMINAL OF SELW RATE CONTROL CODE
SR<0>
SR<1>
SR<2>
60
61
IC
62
INPUT TERMINAL OF IMPEDANCE CONTROL CODE

FIG. 24

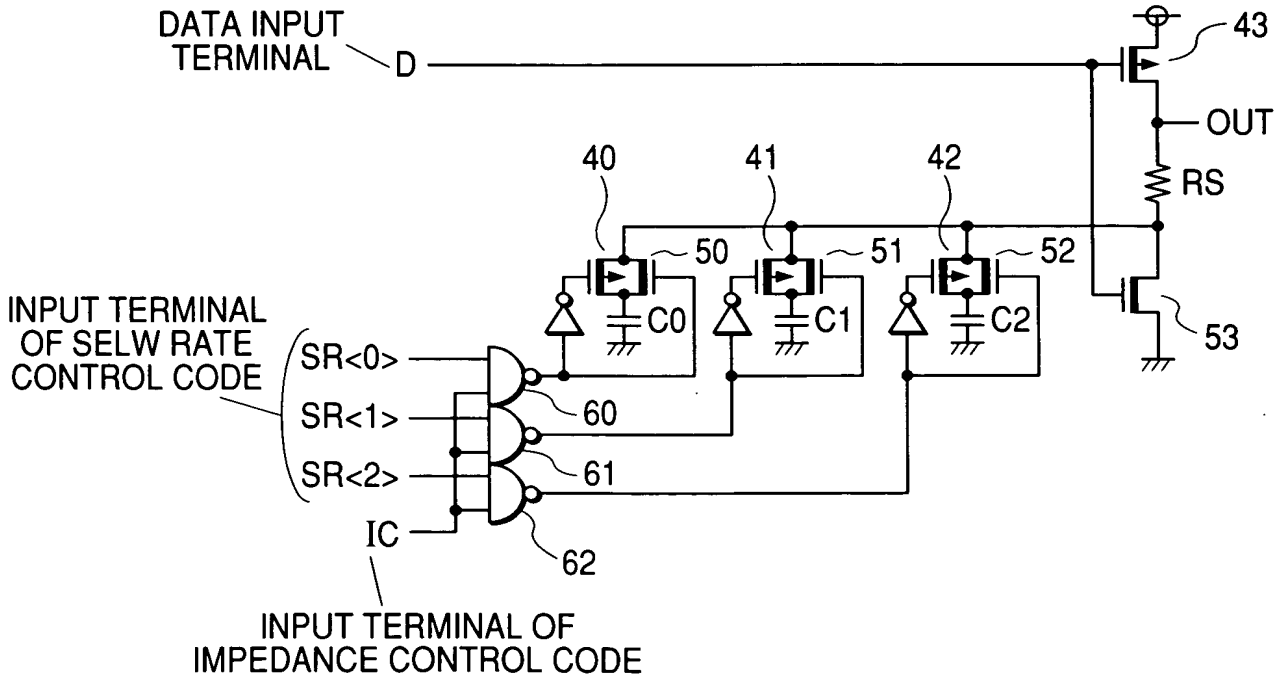

DATA INPUT TERMINAL
D
43
OUT
RS
40
41
42
50
51
52
C0
C1
C2
53
INPUT TERMINAL OF SELW RATE CONTROL CODE
SR<0>
SR<1>
SR<2>
60
61
IC
62
INPUT TERMINAL OF IMPEDANCE CONTROL CODE

FIG. 25

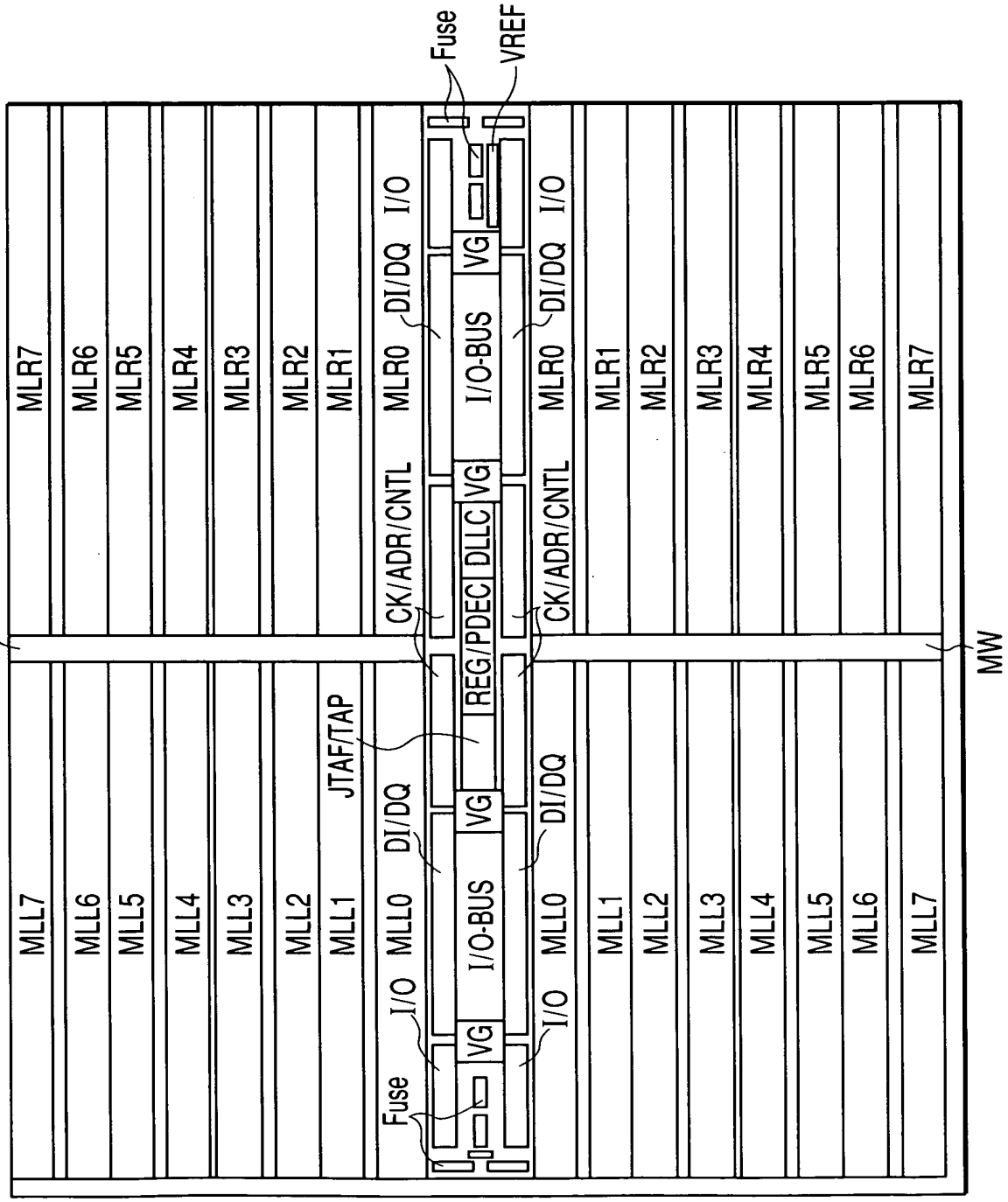

MW
MLR7
MLR6
MLR5
MLR4
MLR3
MLR2
MLR1
MLR0
DI/DQ
I/O
Fuse
VREF
VG
I/O-BUS
CK/ADR/CNTL
REG/PDEC
DLLC
MLL7
MLL6
MLL5
MLL4
MLL3
MLL2
MLL1
MLL0
JTAF/TAP
MW

FIG. 26

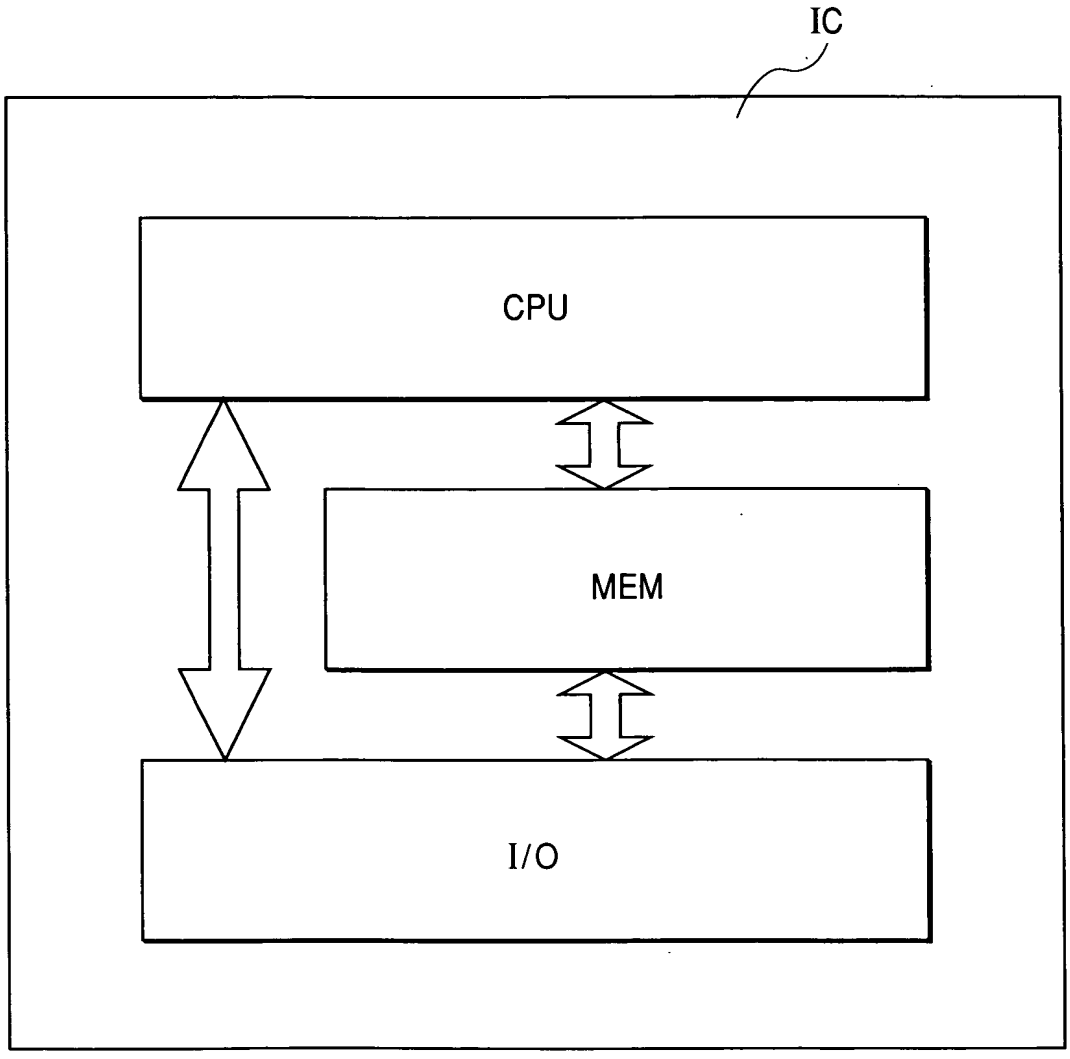


FIG. 27

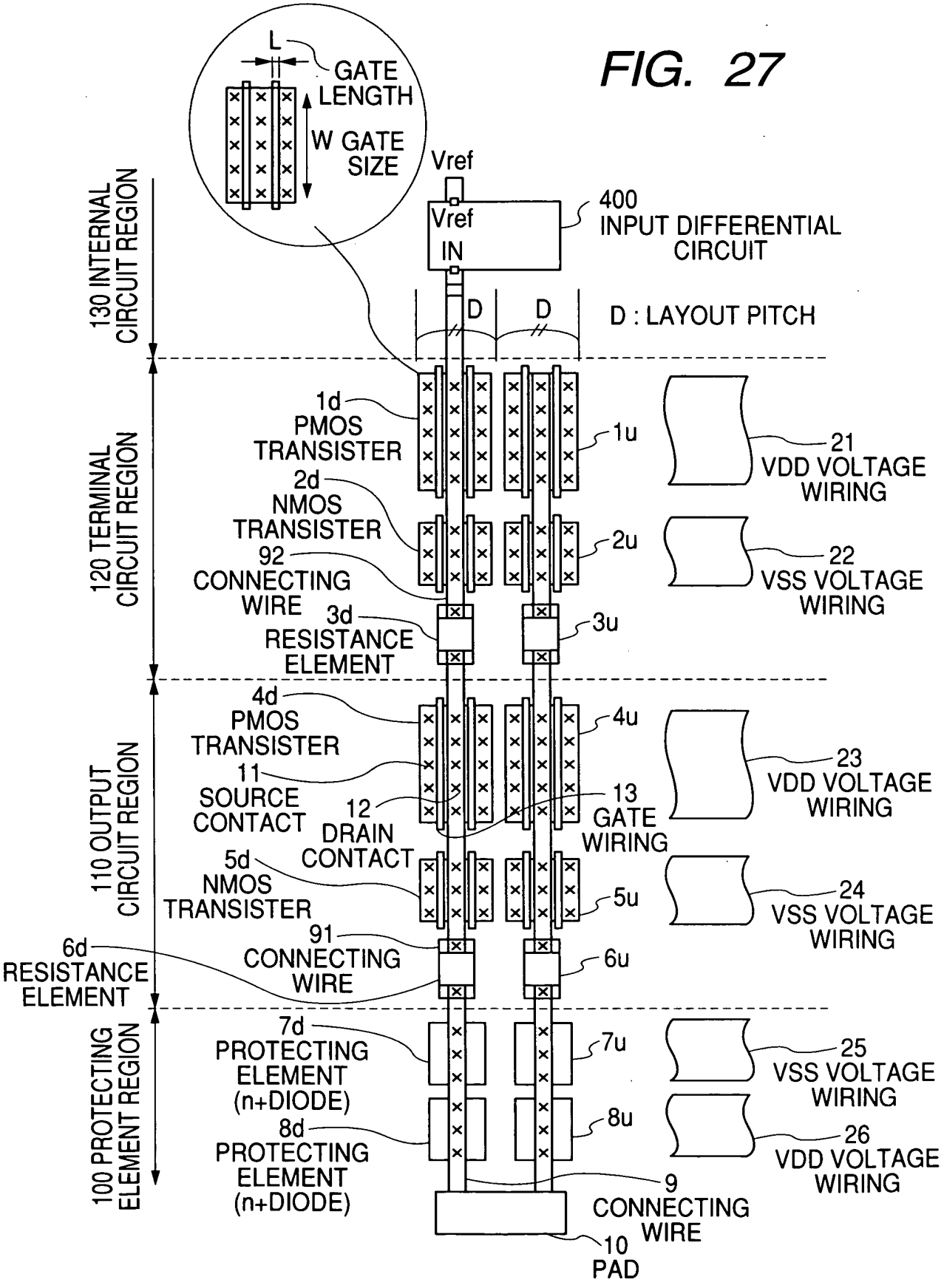

L
GATE LENGTH
W GATE SIZE
Vref
Vref
IN
400
INPUT DIFFERENTIAL CIRCUIT
D
D
D : LAYOUT PITCH
130 INTERNAL CIRCUIT REGION
120 TERMINAL CIRCUIT REGION
110 OUTPUT CIRCUIT REGION
100 PROTECTING ELEMENT REGION
1d
PMOS TRANSISTER
1u
2d
NMOS TRANSISTER
2u
92
CONNECTING WIRE
3d
RESISTANCE ELEMENT
3u
4d
PMOS TRANSISTER
4u
11
SOURCE CONTACT
12
DRAIN CONTACT
13
GATE WIRING
5d
NMOS TRANSISTER
5u
91
CONNECTING WIRE
6d
RESISTANCE ELEMENT
6u
7d
PROTECTING ELEMENT (n+DIODE)
7u
8d
PROTECTING ELEMENT (n+DIODE)
8u
9
CONNECTING WIRE
10
PAD
21
VDD VOLTAGE WIRING
22
VSS VOLTAGE WIRING
23
VDD VOLTAGE WIRING
24
VSS VOLTAGE WIRING
25
VSS VOLTAGE WIRING
26
VDD VOLTAGE WIRING

FIG. 28

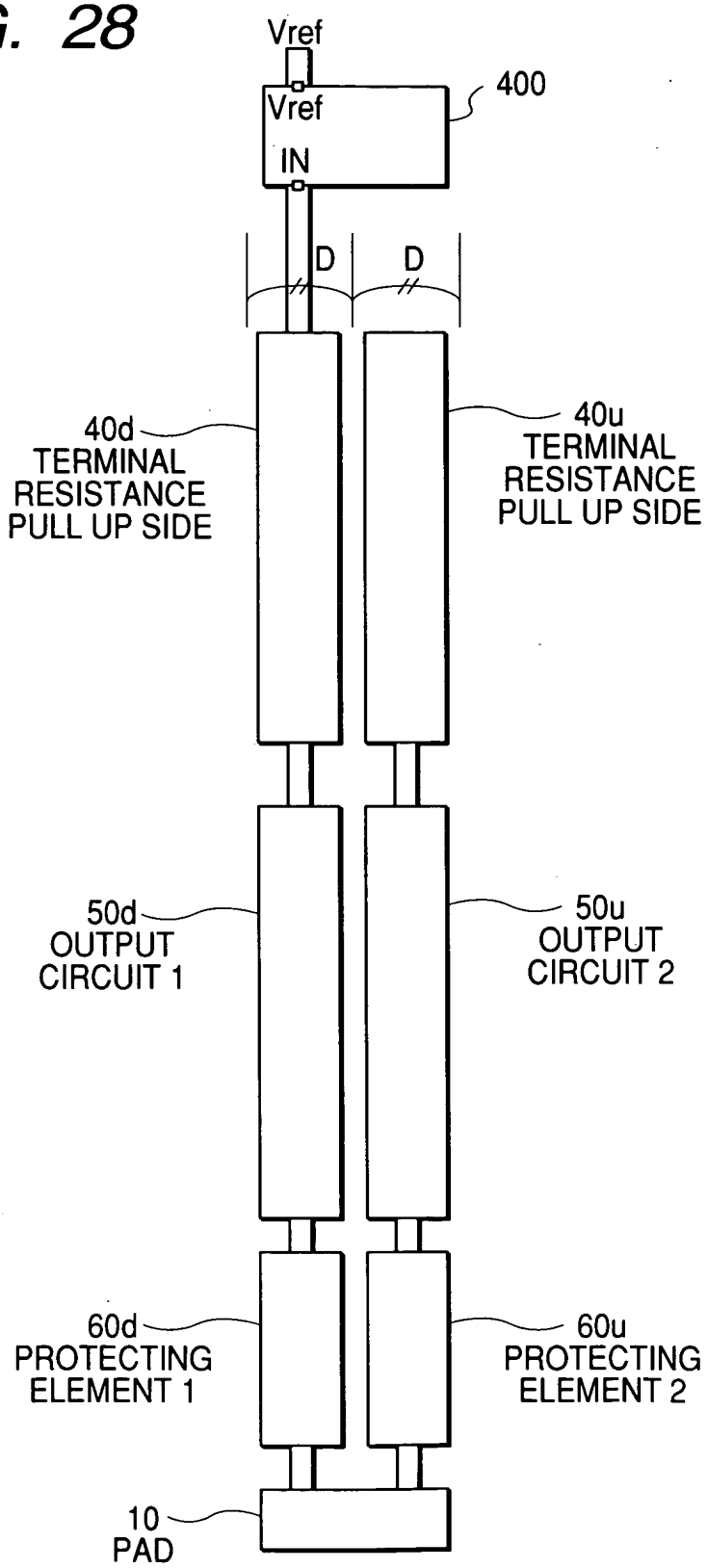

Vref
Vref
IN
400
D
D
40d
TERMINAL
RESISTANCE
PULL UP SIDE
40u
TERMINAL
RESISTANCE
PULL UP SIDE
50d
OUTPUT
CIRCUIT 1
50u
OUTPUT
CIRCUIT 2
60d
PROTECTING
ELEMENT 1
60u
PROTECTING
ELEMENT 2
10
PAD

FIG. 29

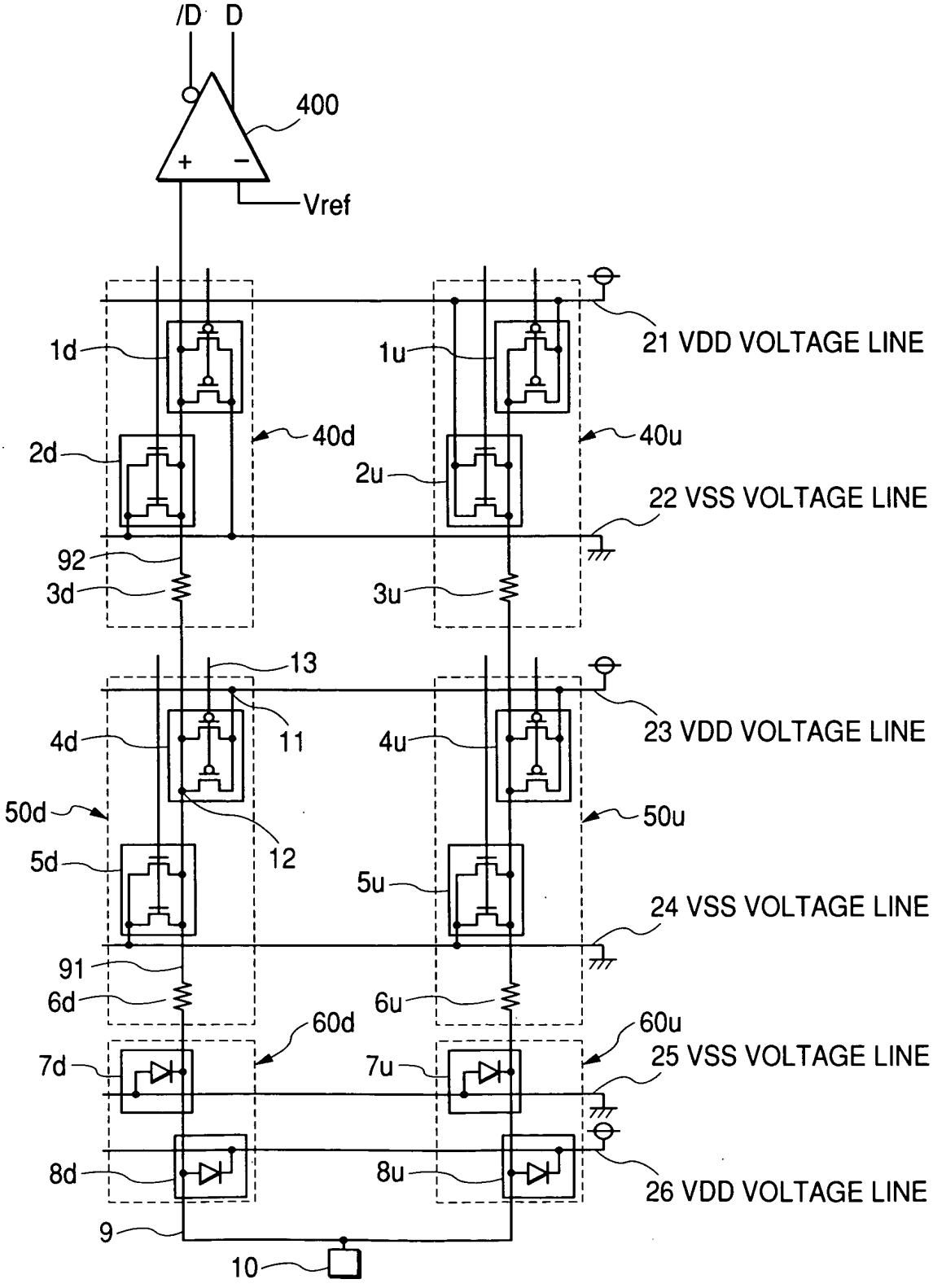

/D
D
400
+
−
Vref
1d
1u
21 VDD VOLTAGE LINE
2d
40d
2u
40u
22 VSS VOLTAGE LINE
92
3d
3u
13
4d
11
4u
23 VDD VOLTAGE LINE
50d
50u
5d
12
5u
24 VSS VOLTAGE LINE
91
6d
6u
60d
60u
7d
7u
25 VSS VOLTAGE LINE
8d
8u
26 VDD VOLTAGE LINE
9
10

FIG. 30

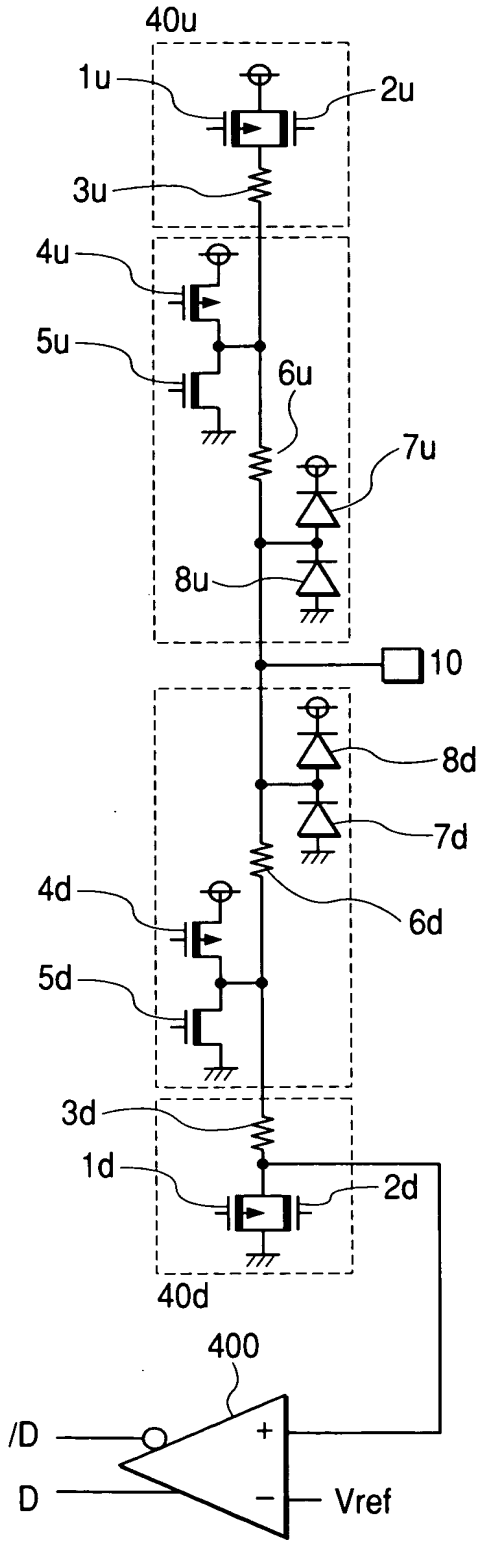


FIG. 31

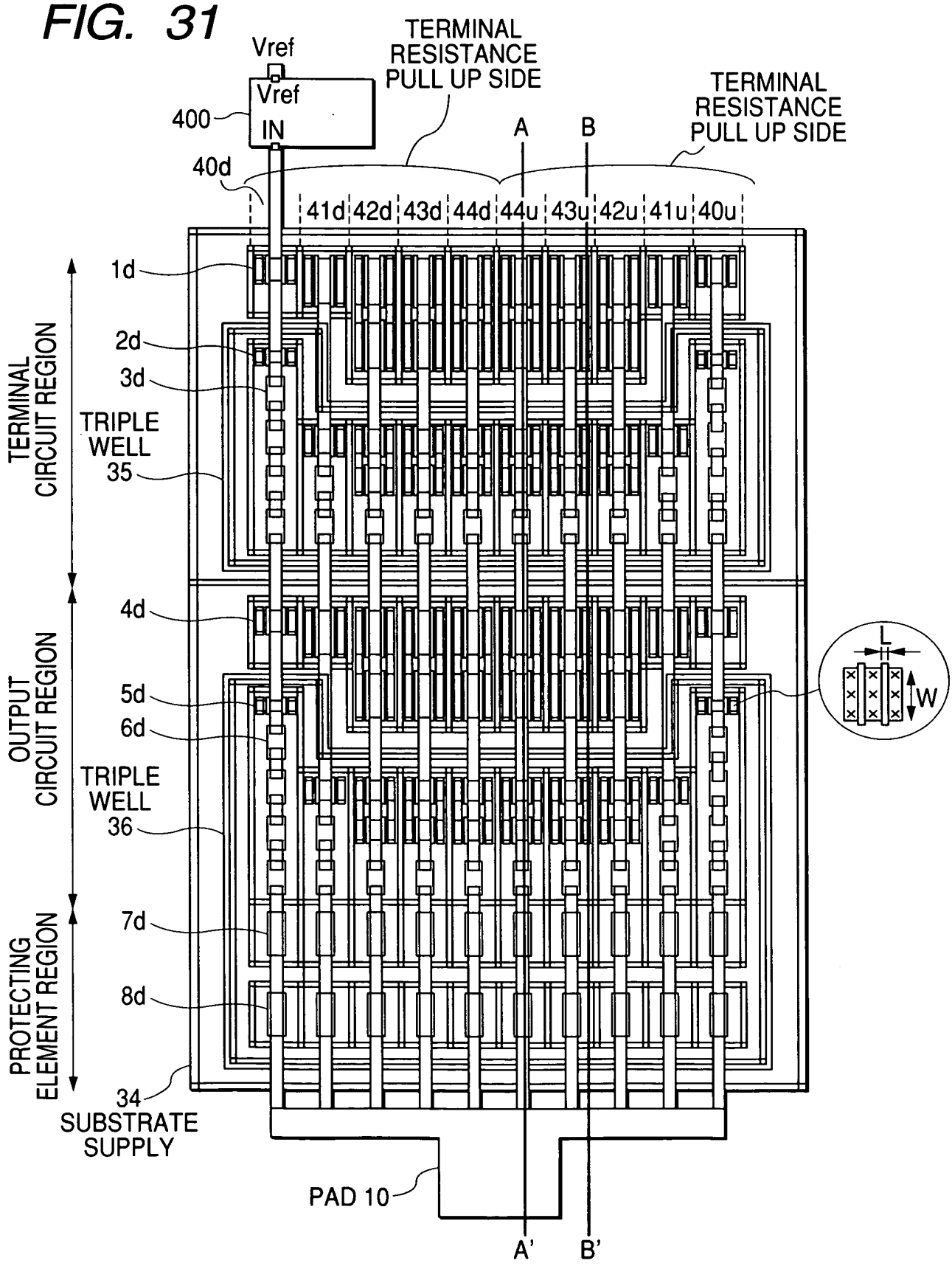

Vref
Vref
IN
400
TERMINAL RESISTANCE PULL UP SIDE
TERMINAL RESISTANCE PULL UP SIDE
A
B
40d
41d 42d 43d 44d 44u 43u 42u 41u 40u
1d
2d
3d
TRIPLE WELL
35
4d
5d
6d
TRIPLE WELL
36
7d
8d
34
SUBSTRATE SUPPLY
TERMINAL CIRCUIT REGION
OUTPUT CIRCUIT REGION
PROTECTING ELEMENT REGION
PAD 10
A'
B'
L
W

FIG. 32

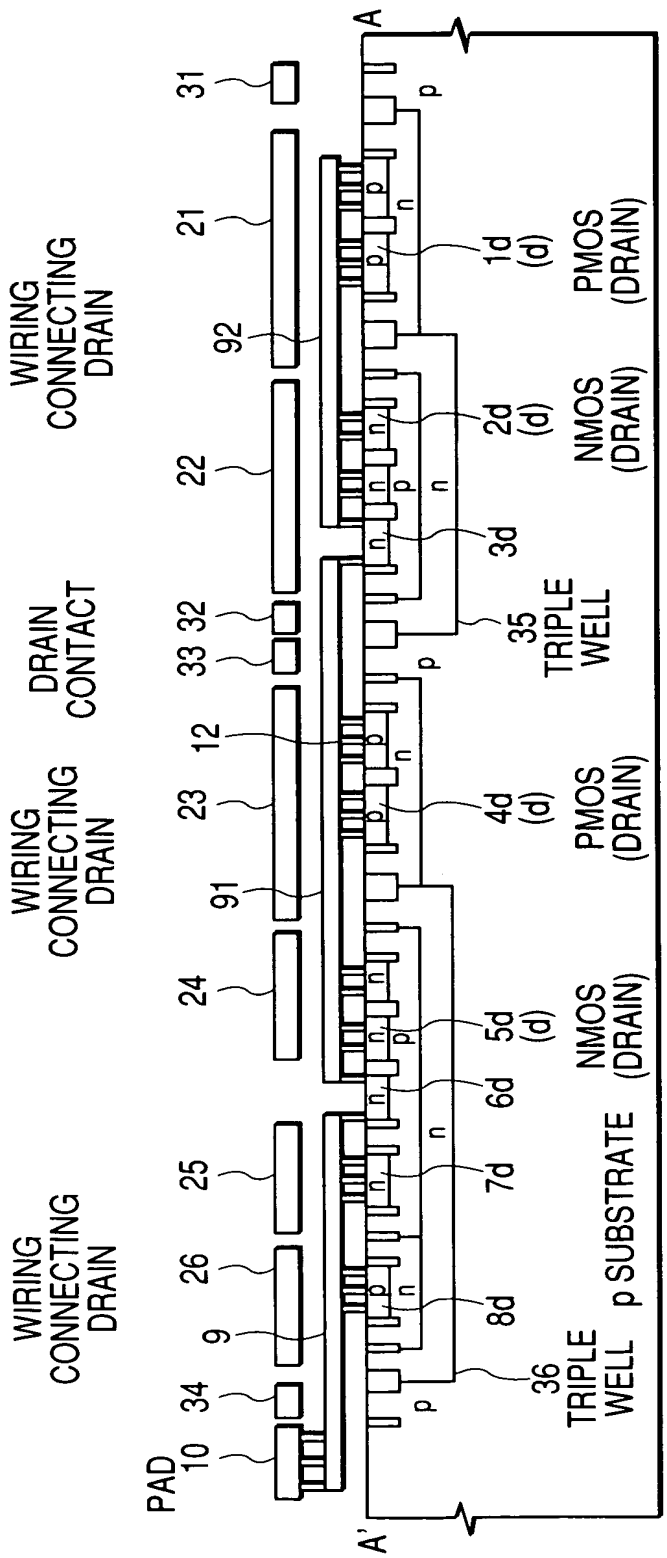

WIRING CONNECTING DRAIN
DRAIN CONTACT
WIRING CONNECTING DRAIN
WIRING CONNECTING DRAIN
PAD
10
34
9
26
25
24
91
23
12
33
32
92
22
21
31
A
A'
TRIPLE WELL
p SUBSTRATE
NMOS (DRAIN)
PMOS (DRAIN)
NMOS (DRAIN)
PMOS (DRAIN)
TRIPLE WELL
36
8d
7d
6d
5d (d)
4d (d)
3d
2d (d)
1d (d)
35
n
p

FIG. 33

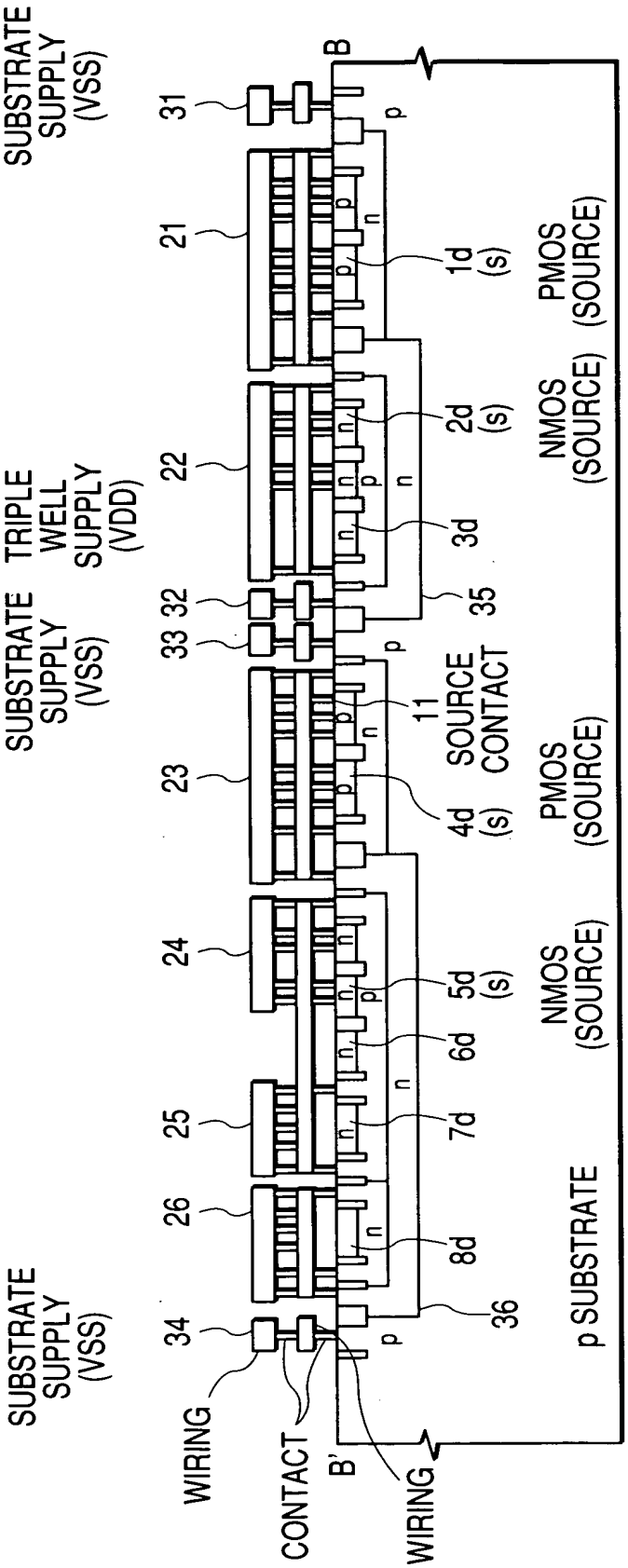

SUBSTRATE SUPPLY (VSS)
TRIPLE WELL SUPPLY (VDD)
SUBSTRATE SUPPLY (VSS)
SUBSTRATE SUPPLY (VSS)
31
21
22
32
33
23
24
25
26
34
B
B'
1d (s)
2d (s)
3d
35
11 SOURCE CONTACT
4d (s)
5d (s)
6d
7d
8d
36
PMOS (SOURCE)
NMOS (SOURCE)
PMOS (SOURCE)
NMOS (SOURCE)
p SUBSTRATE
WIRING
CONTACT
WIRING

FIG. 34

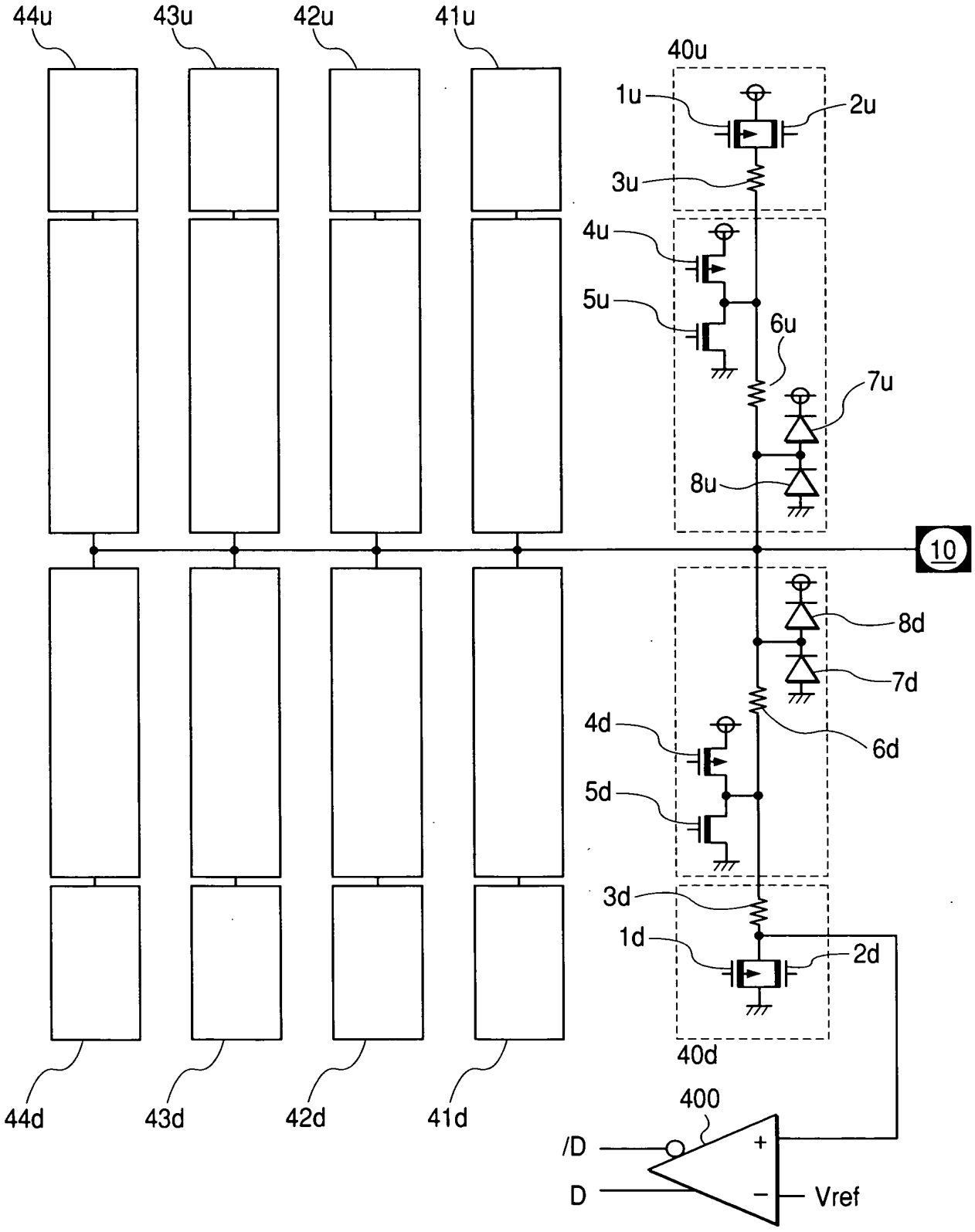

44u
43u
42u
41u
40u
1u
2u
3u
4u
5u
6u
7u
8u
10
8d
7d
6d
4d
5d
3d
1d
2d
40d
400
/D
D
+
−
Vref
44d
43d
42d
41d

FIG. 35

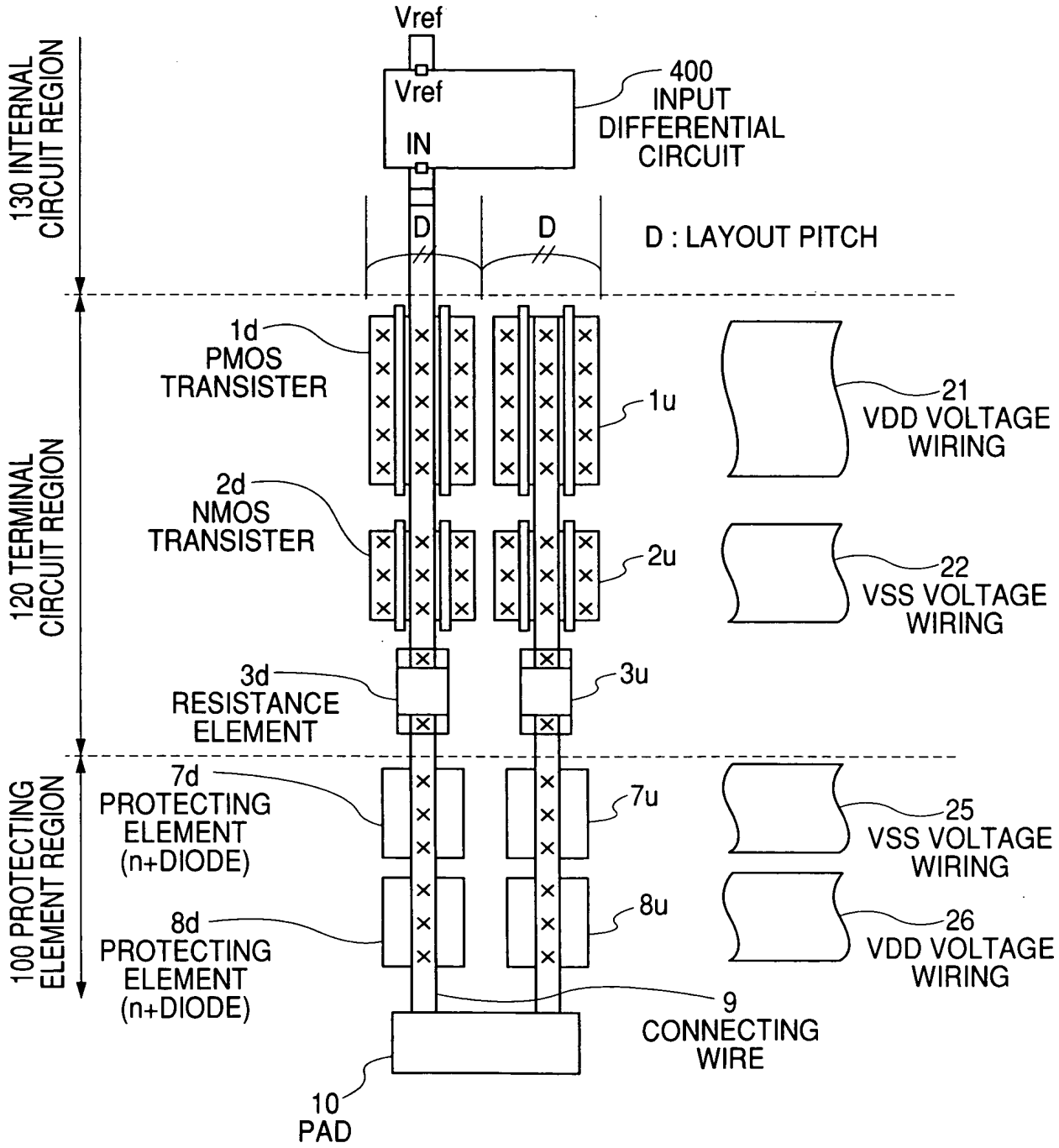

Vref
Vref
IN
400
INPUT
DIFFERENTIAL
CIRCUIT
D
D
D : LAYOUT PITCH
130 INTERNAL
CIRCUIT REGION
120 TERMINAL
CIRCUIT REGION
100 PROTECTING
ELEMENT REGION
1d
PMOS
TRANSISTER
1u
2d
NMOS
TRANSISTER
2u
3d
RESISTANCE
ELEMENT
3u
7d
PROTECTING
ELEMENT
(n+DIODE)
7u
8d
PROTECTING
ELEMENT
(n+DIODE)
8u
9
CONNECTING
WIRE
10
PAD
21
VDD VOLTAGE
WIRING
22
VSS VOLTAGE
WIRING
25
VSS VOLTAGE
WIRING
26
VDD VOLTAGE
WIRING

FIG. 36

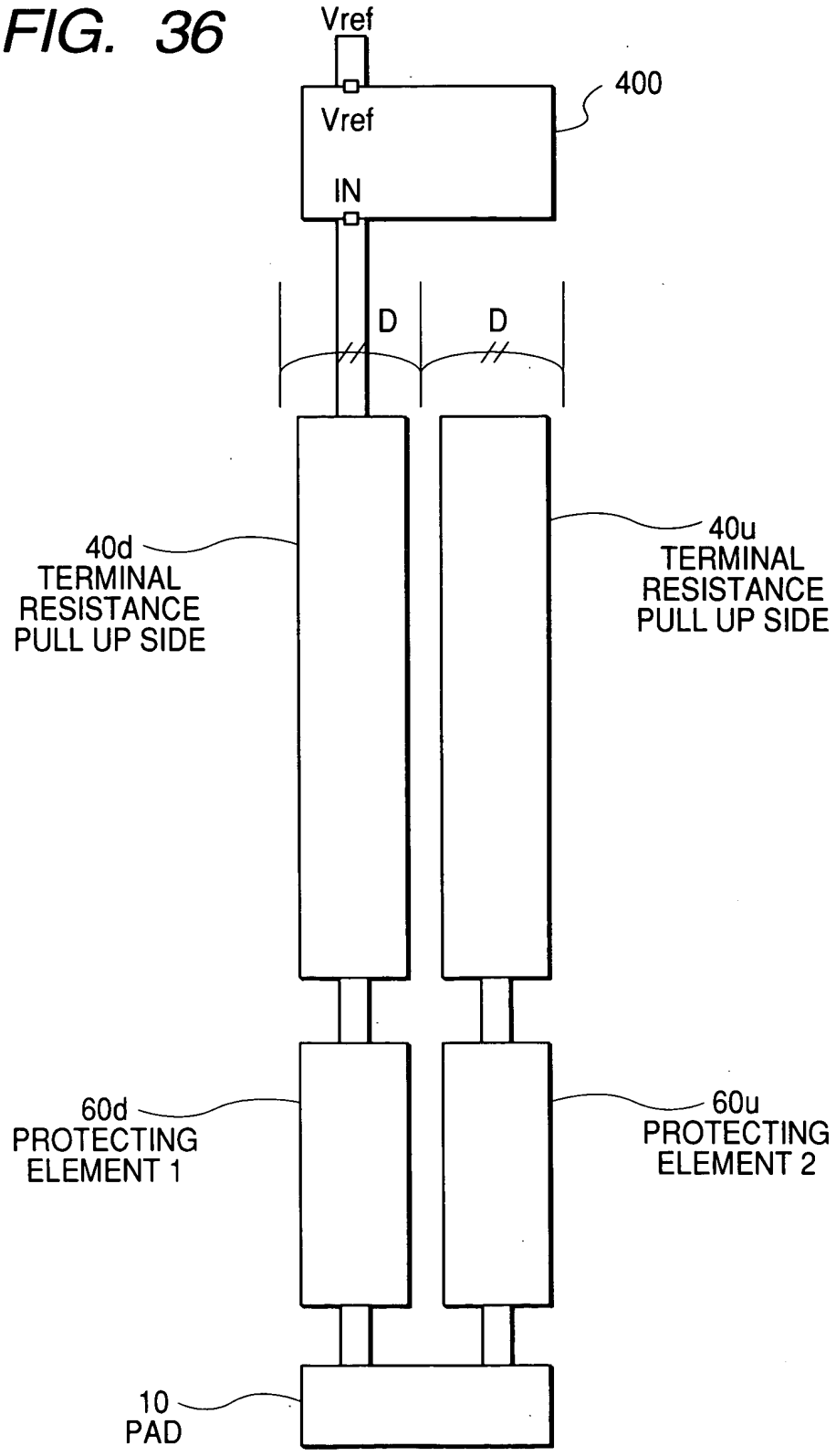

Vref
Vref
400
IN
D
D
40d
TERMINAL
RESISTANCE
PULL UP SIDE
40u
TERMINAL
RESISTANCE
PULL UP SIDE
60d
PROTECTING
ELEMENT 1
60u
PROTECTING
ELEMENT 2
10
PAD

FIG. 37

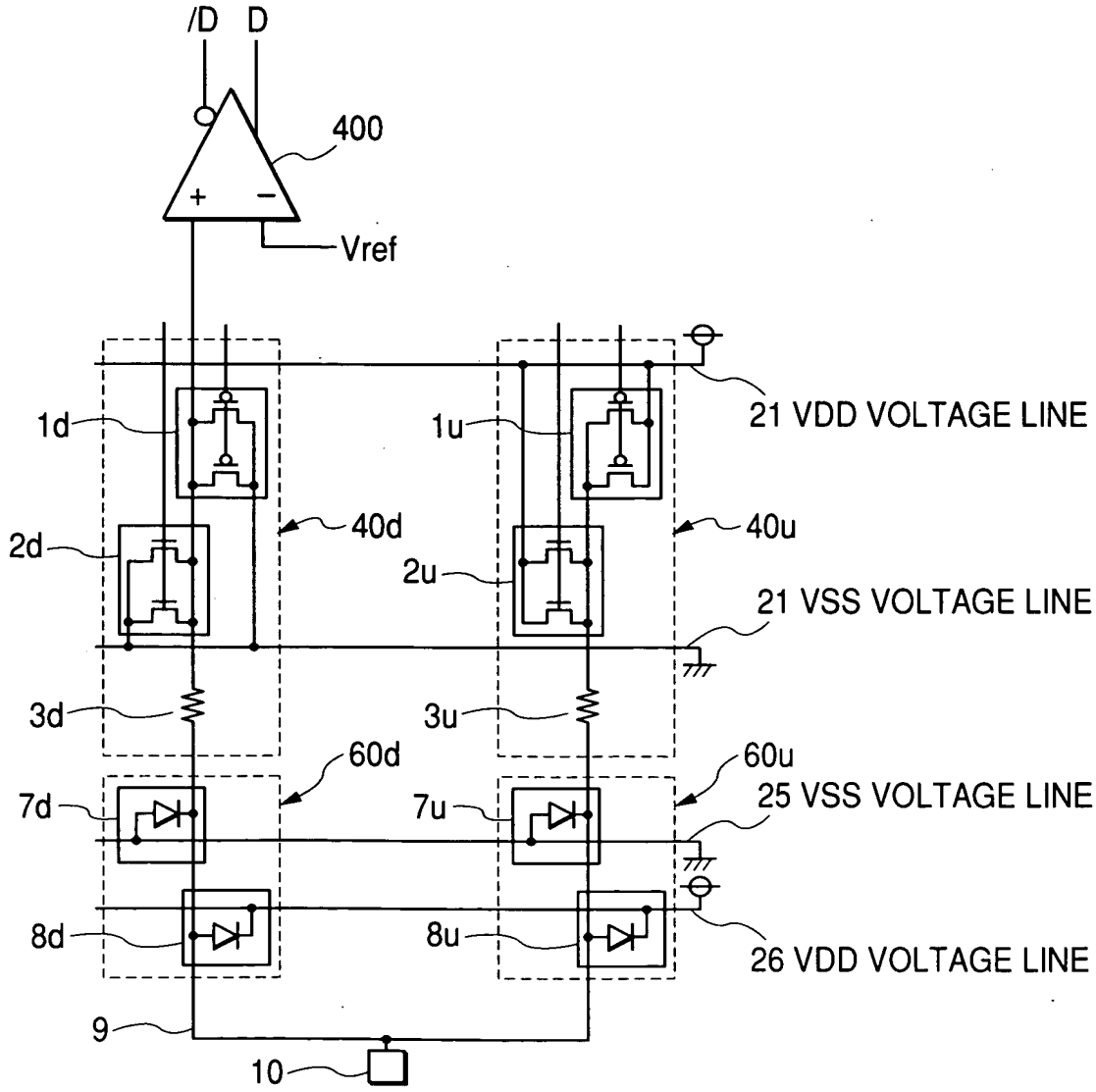

/D
D
400
+
−
Vref
1d
1u
21 VDD VOLTAGE LINE
2d
40d
2u
40u
21 VSS VOLTAGE LINE
3d
3u
60d
60u
7d
7u
25 VSS VOLTAGE LINE
8d
8u
26 VDD VOLTAGE LINE
9
10

FIG. 38

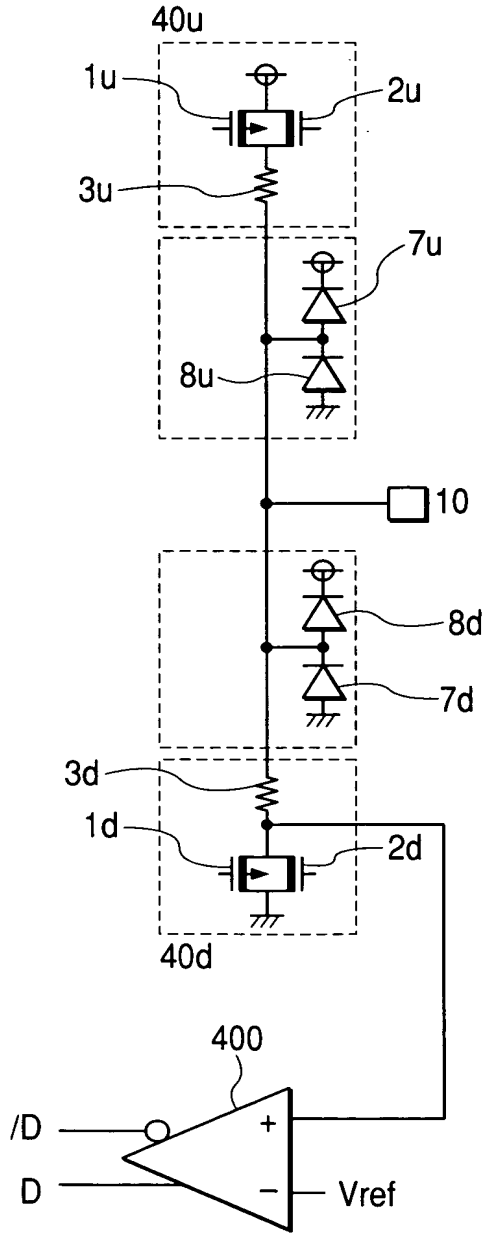


FIG. 39

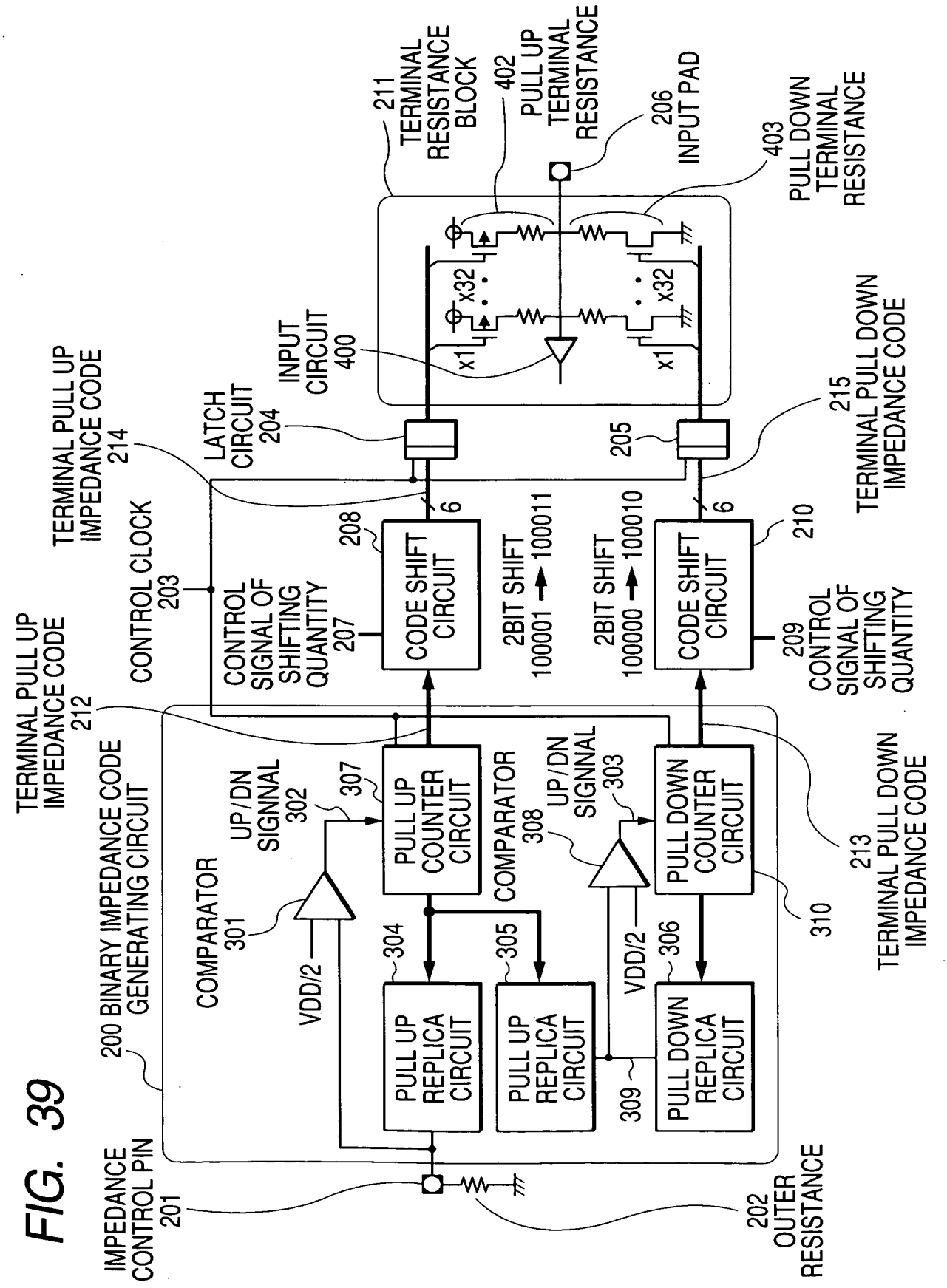

IMPEDANCE CONTROL PIN 201
200 BINARY IMPEDANCE CODE GENERATING CIRCUIT
202 OUTER RESISTANCE
TERMINAL PULL UP IMPEDANCE CODE 212
213 TERMINAL PULL DOWN IMPEDANCE CODE
COMPARATOR 301
UP/DN SIGNNAL 302
307
PULL UP COUNTER CIRCUIT
COMPARATOR 308
UP/DN SIGNNAL 303
PULL DOWN COUNTER CIRCUIT
310
VDD/2
304
305
306
309
PULL UP REPLICA CIRCUIT
PULL UP REPLICA CIRCUIT
PULL DOWN REPLICA CIRCUIT
CONTROL CLOCK 203
CONTROL SIGNAL OF SHIFTING QUANTITY 207
208
CODE SHIFT CIRCUIT
6
2BIT SHIFT 100001 → 100011
2BIT SHIFT 100000 → 100010
CODE SHIFT CIRCUIT
6
210
209 CONTROL SIGNAL OF SHIFTING QUANTITY
TERMINAL PULL UP IMPEDANCE CODE 214
LATCH CIRCUIT 204
205
215 TERMINAL PULL DOWN IMPEDANCE CODE
INPUT CIRCUIT 400
x1
x32
x1
x32
211 TERMINAL RESISTANCE BLOCK
402 PULL UP TERMINAL RESISTANCE
206 INPUT PAD
403 PULL DOWN TERMINAL RESISTANCE

FIG. 40

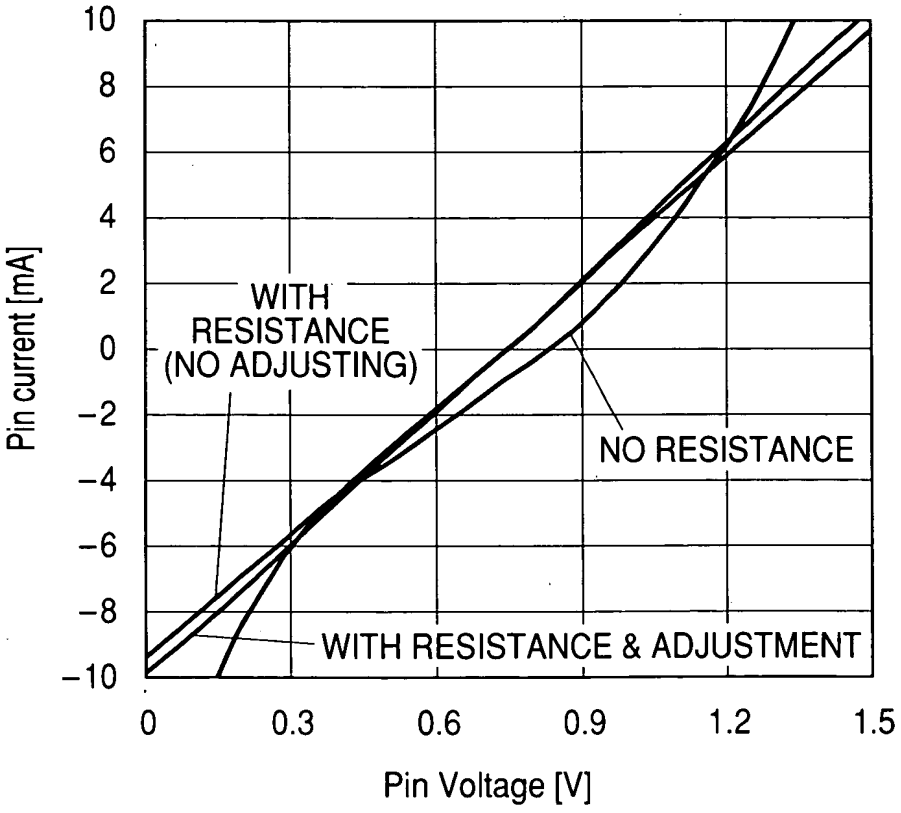

10
8
6
4
2
0
−2
−4
−6
−8
−10
Pin current [mA]
0
0.3
0.6
0.9
1.2
1.5
Pin Voltage [V]
WITH RESISTANCE (NO ADJUSTING)
NO RESISTANCE
WITH RESISTANCE & ADJUSTMENT

FIG. 41

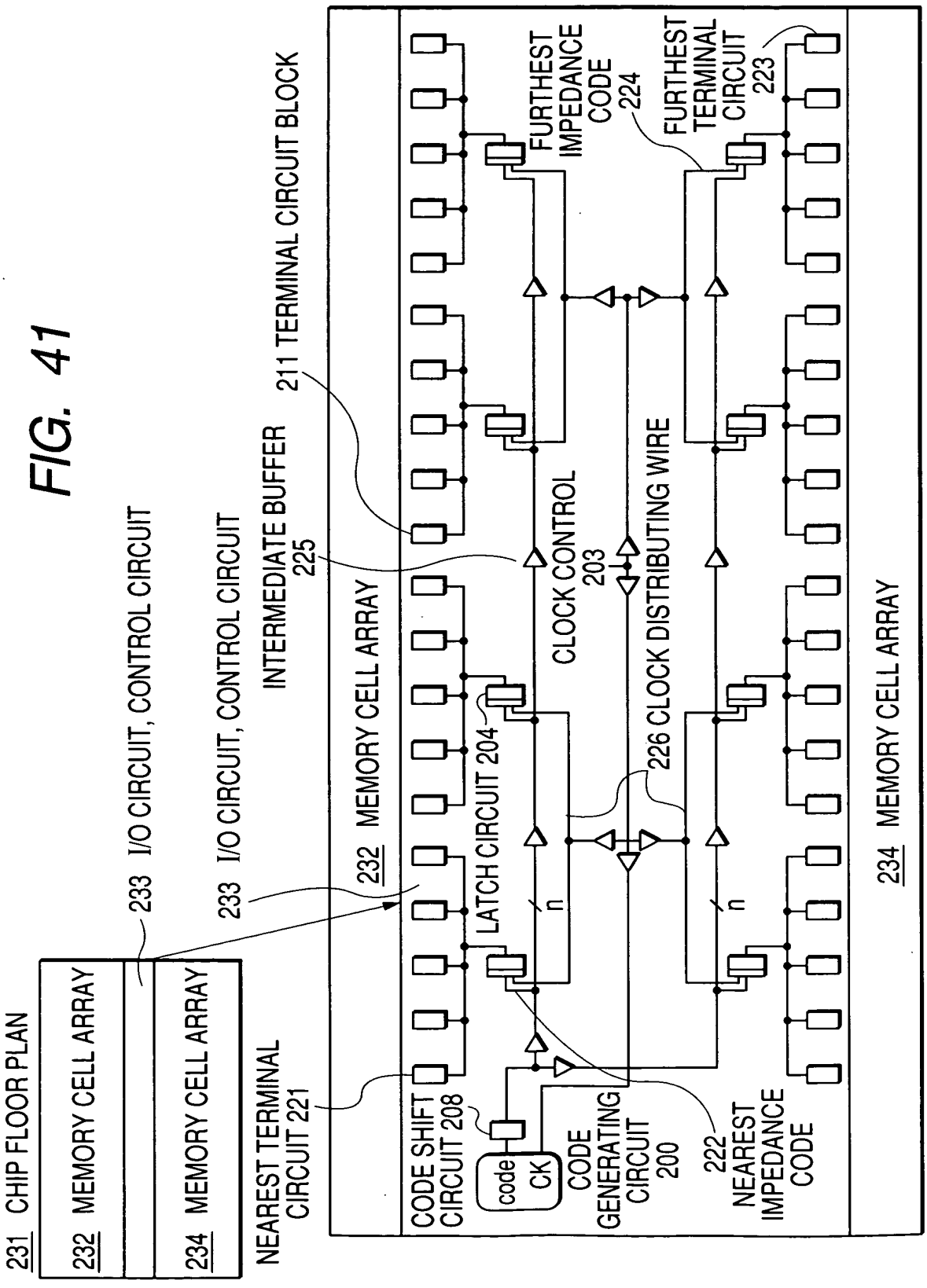

231 CHIP FLOOR PLAN
232 MEMORY CELL ARRAY
234 MEMORY CELL ARRAY
233 I/O CIRCUIT, CONTROL CIRCUIT
233 I/O CIRCUIT, CONTROL CIRCUIT
NEAREST TERMINAL CIRCUIT 221
INTERMEDIATE BUFFER 225
211 TERMINAL CIRCUIT BLOCK
232 MEMORY CELL ARRAY
CODE SHIFT CIRCUIT 208
LATCH CIRCUIT 204
CLOCK CONTROL 203
226 CLOCK DISTRIBUTING WIRE
FURTHEST IMPEDANCE CODE 224
FURTHEST TERMINAL CIRCUIT 223
code
CK
CODE GENERATING CIRCUIT 200
222 NEAREST IMPEDANCE CODE
n
n
234 MEMORY CELL ARRAY

FIG. 42

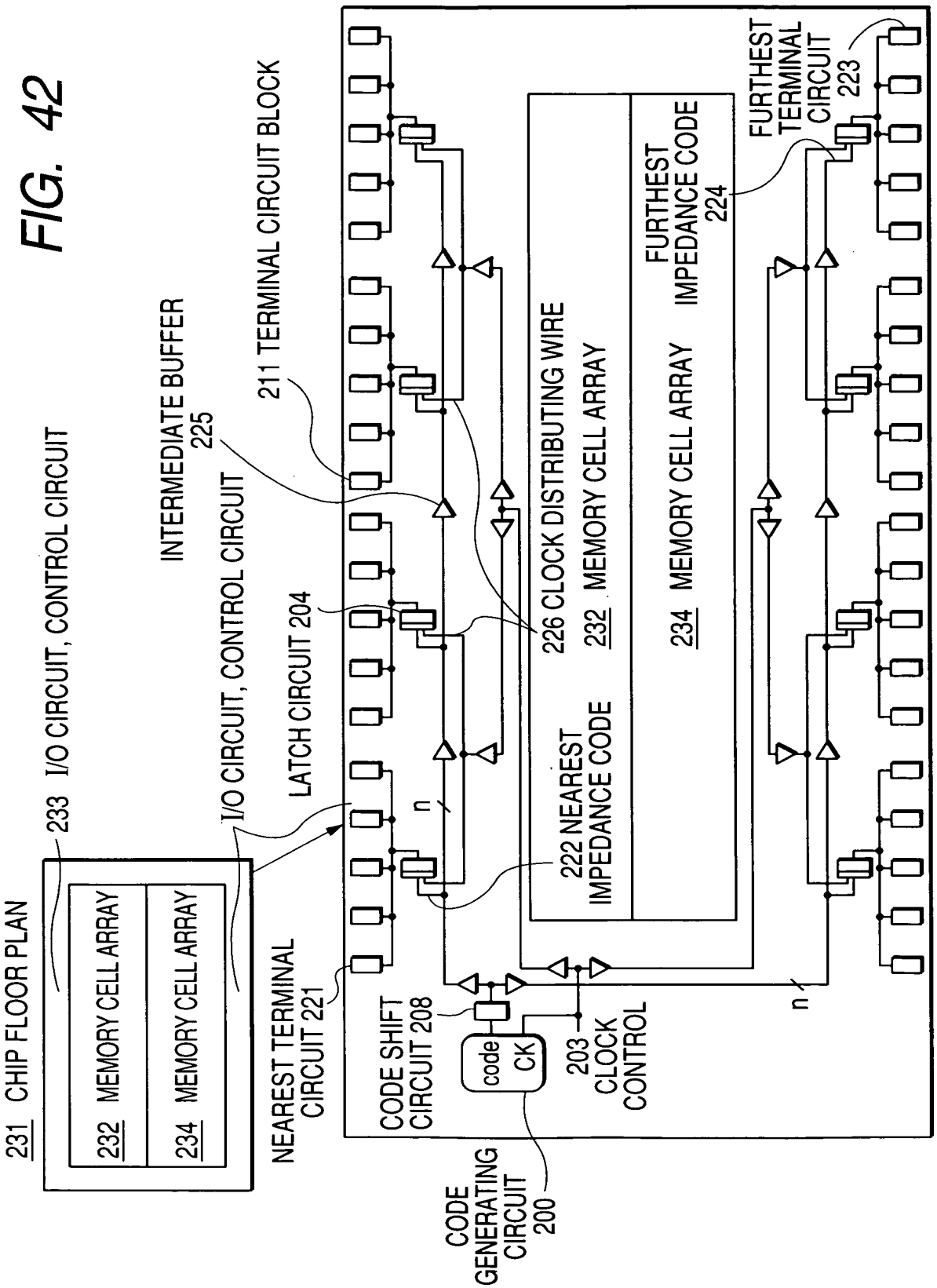

231 CHIP FLOOR PLAN
232 MEMORY CELL ARRAY
234 MEMORY CELL ARRAY
233 I/O CIRCUIT, CONTROL CIRCUIT
I/O CIRCUIT, CONTROL CIRCUIT
INTERMEDIATE BUFFER
225
211 TERMINAL CIRCUIT BLOCK
LATCH CIRCUIT 204
NEAREST TERMINAL CIRCUIT 221
CODE SHIFT CIRCUIT 208
code
CK
CODE GENERATING CIRCUIT 200
203 CLOCK CONTROL
n
n
222 NEAREST IMPEDANCE CODE
226 CLOCK DISTRIBUTING WIRE
232 MEMORY CELL ARRAY
234 MEMORY CELL ARRAY
FURTHEST IMPEDANCE CODE 224
FURTHEST TERMINAL CIRCUIT 223

FIG. 43

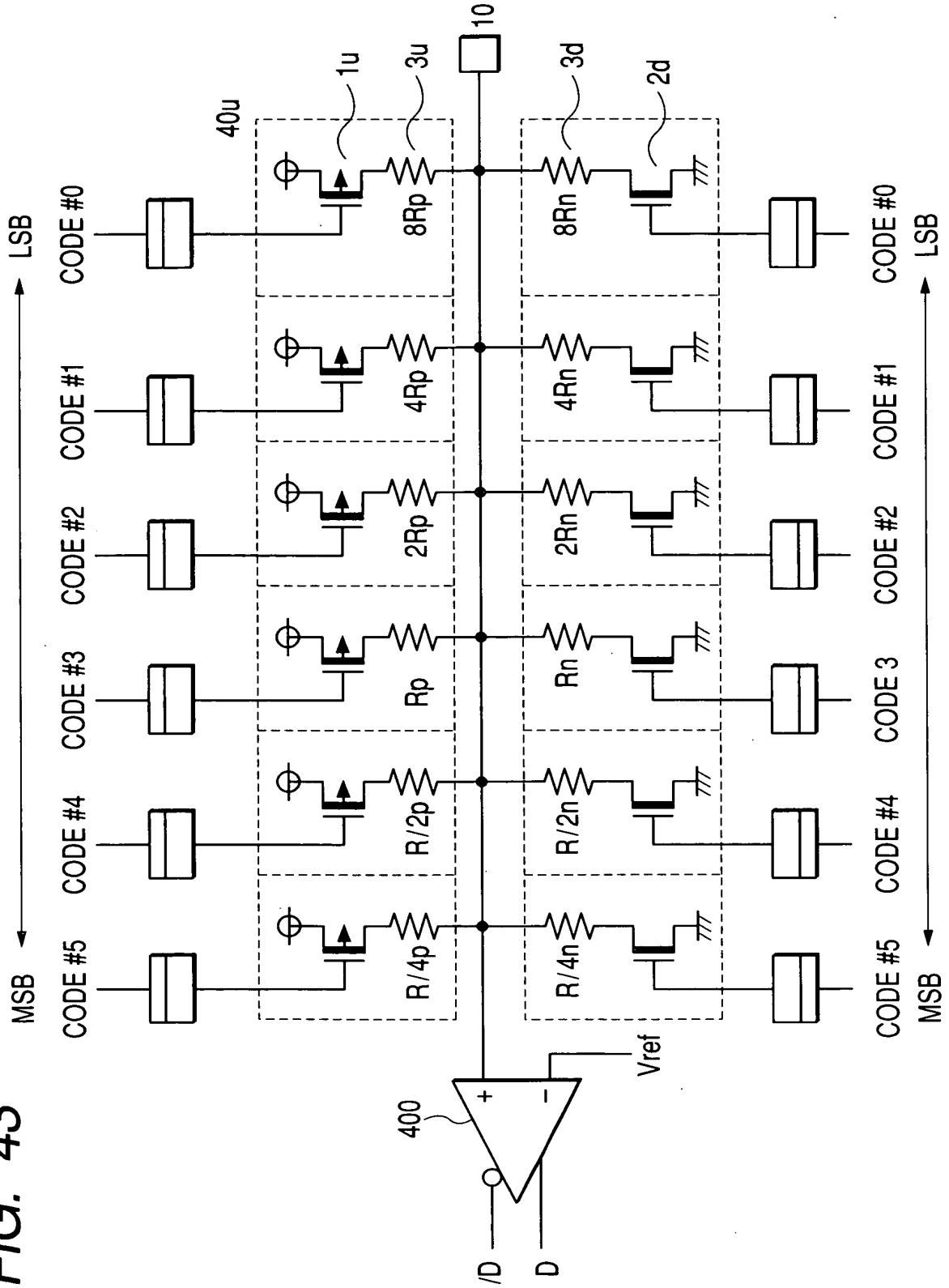

10
40u
1u
3u
3d
2d
8Rp
8Rn
4Rp
4Rn
2Rp
2Rn
Rp
Rn
R/2p
R/2n
R/4p
R/4n
LSB
MSB
CODE #0
CODE #1
CODE #2
CODE #3
CODE #4
CODE #5
CODE 3
400
Vref
/D
D
+
-

FIG. 44

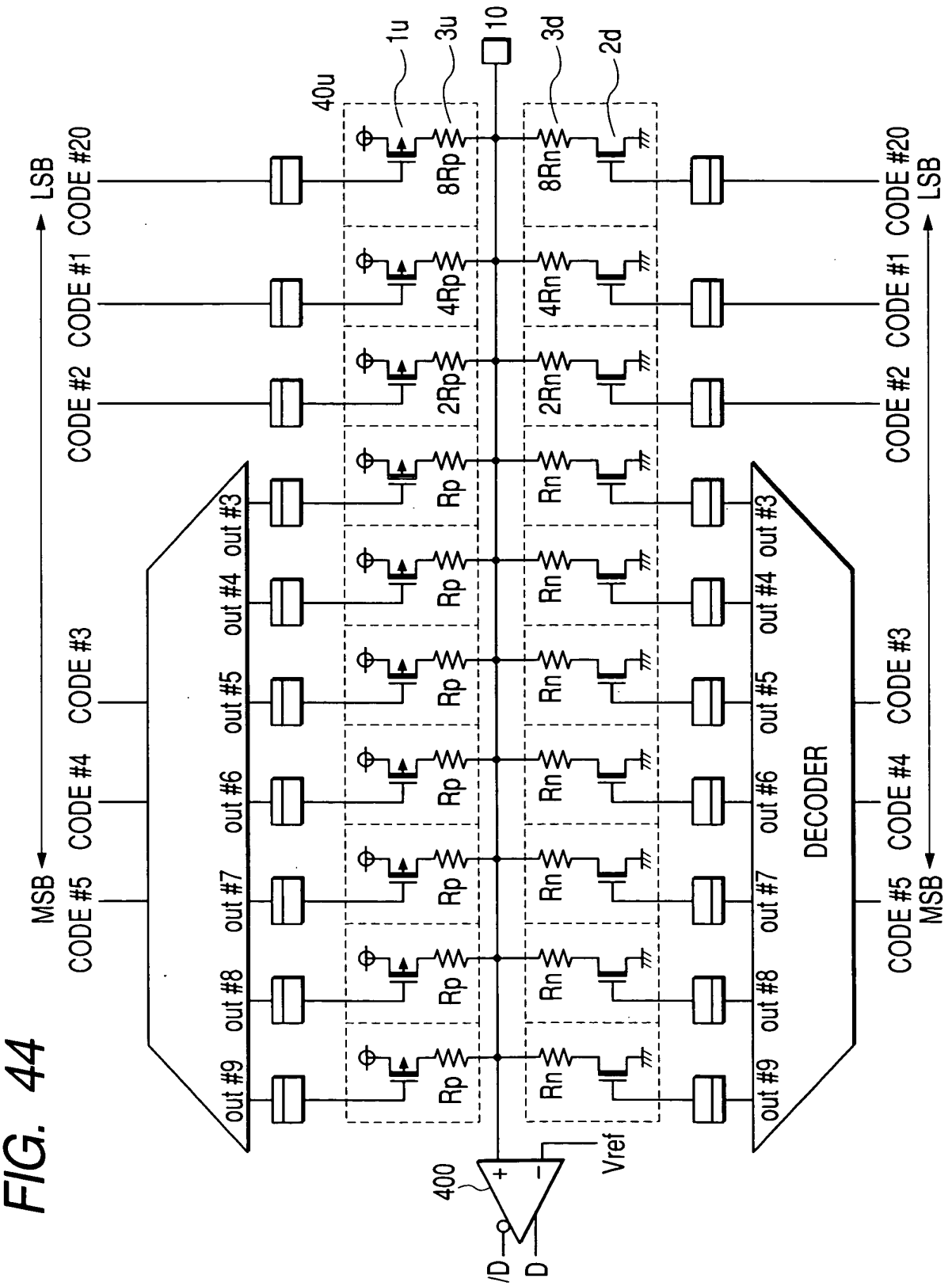

LSB
MSB
CODE #20
CODE #1
CODE #2
CODE #3
CODE #4
CODE #5
40u
1u
3u
10
3d
2d
8Rp
4Rp
2Rp
Rp
8Rn
4Rn
2Rn
Rn
out #3
out #4
out #5
out #6
out #7
out #8
out #9
DECODER
400
Vref
/D
D

FIG. 45

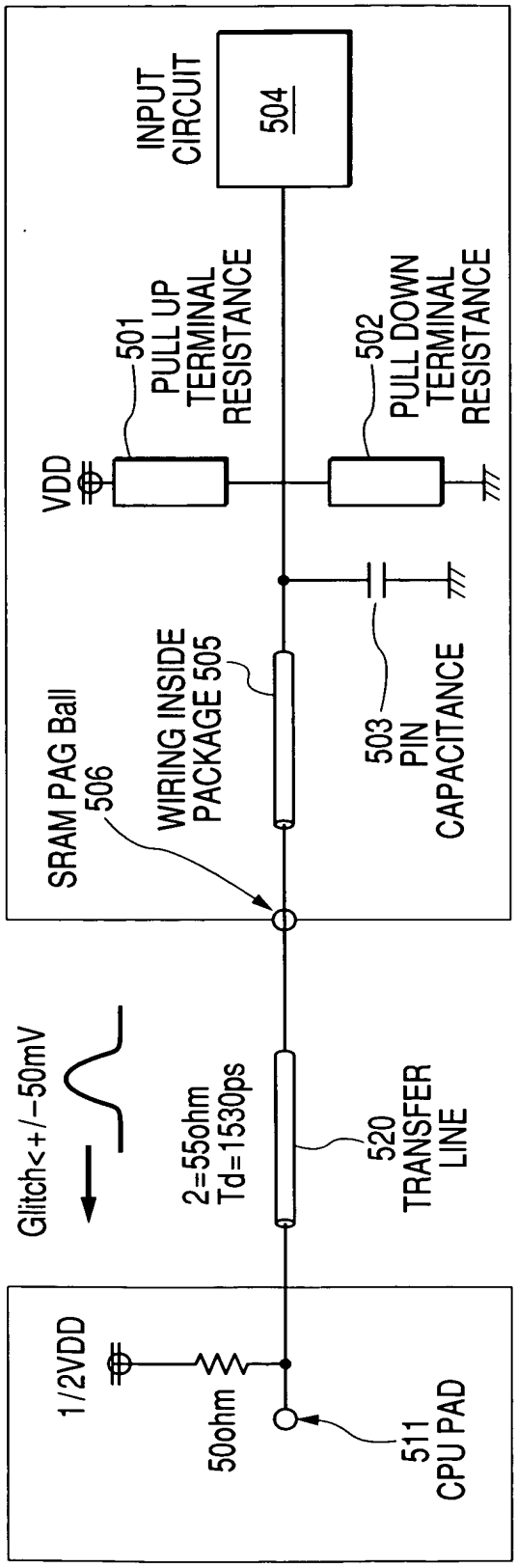

INPUT CIRCUIT
504
501 PULL UP TERMINAL RESISTANCE
502 PULL DOWN TERMINAL RESISTANCE
VDD
SRAM PAG Ball
506
WIRING INSIDE PACKAGE 505
503 PIN CAPACITANCE
Glitch<+/−50mV
2=55ohm Td=1530ps
520 TRANSFER LINE
1/2VDD
50ohm
511 CPU PAD

FIG. 46

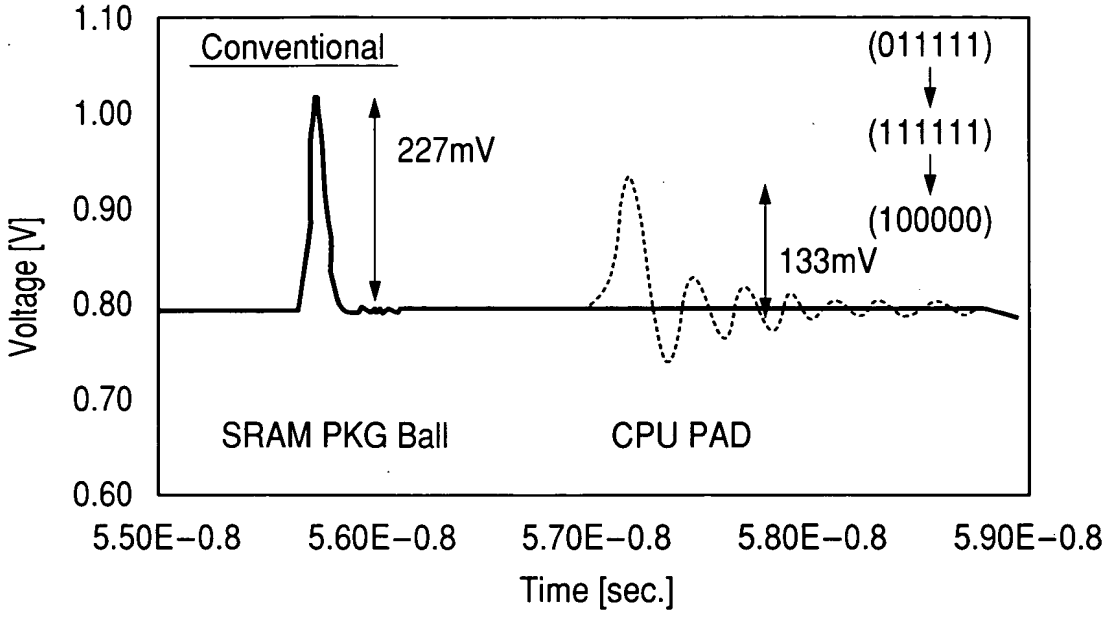
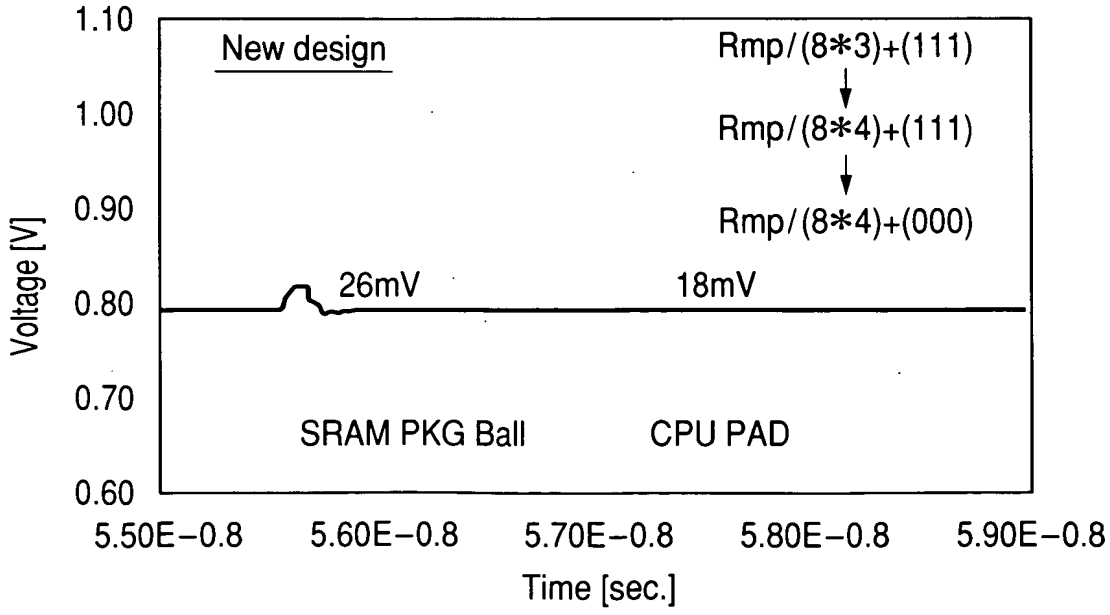

Conventional
(011111)
(111111)
(100000)
227mV
133mV
1.10
1.00
0.90
0.80
0.70
0.60
Voltage [V]
SRAM PKG Ball
CPU PAD
5.50E−0.8
5.60E−0.8
5.70E−0.8
5.80E−0.8
5.90E−0.8
Time [sec.]

FIG. 47


New design
Rmp/(8*3)+(111)
Rmp/(8*4)+(111)
Rmp/(8*4)+(000)
26mV
18mV
1.10
1.00
0.90
0.80
0.70
0.60
Voltage [V]
SRAM PKG Ball
CPU PAD
5.50E−0.8
5.60E−0.8
5.70E−0.8
5.80E−0.8
5.90E−0.8
Time [sec.]